A New VMEbus Technology Infusion

Tempe Bridge: The High Speed VMEbus ASIC from Motorola

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VMEbus Performance Evolution

MOTOROLA VME 1981 - 2001

Date	Backplane	Protocol	Data Transfer Protocol	Theoretical Performance	Achievable Performance
1981	VME 3-row P1 and P2	BLT	Asynchronous 32-bit 4-edge handshake	40	~20
1989	VME64	MBLT	Asynchronous 64-bit 4-edge handshake	80	~40
1995	VME64x 5-row P1 and P2	2eVME	Asynchronous 64-bit 2-edge handshake	160	~70
1999	No change	2eSST	Synchronous 64-bit no handshake	320	~320

What is 2eSST?

- A VITA trial use standard (VITA 1.5)
- 2eSST = 2 edge Source Synchronous Transfer.
- 2e = data is driven on both the falling and the rising edges of a strobe, or clock, permitting the transfer of two bits of data per each clock.
- Source Synchronous = the strobe, which is used as a transfer clock, is driven by the sender of the data without requiring an acknowledge signal from the receiver.

Data Transfer Protocols

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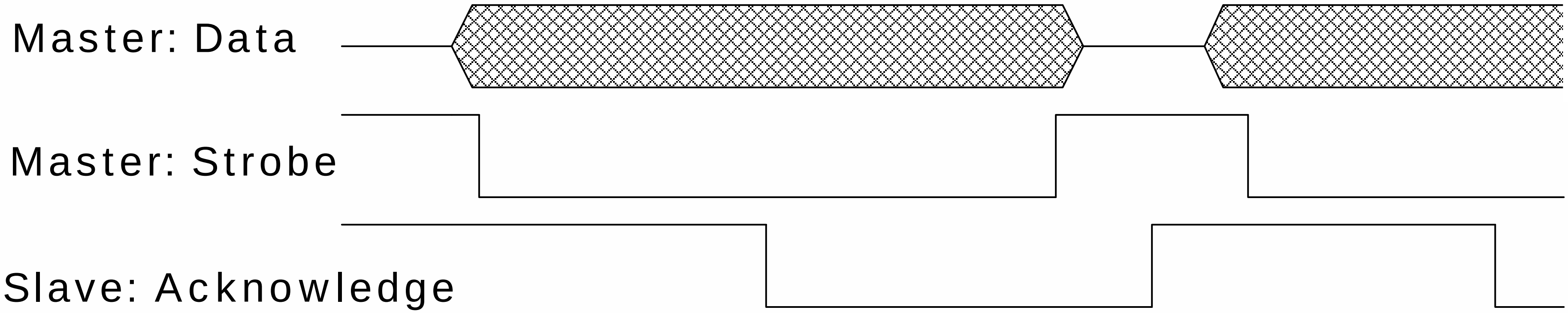
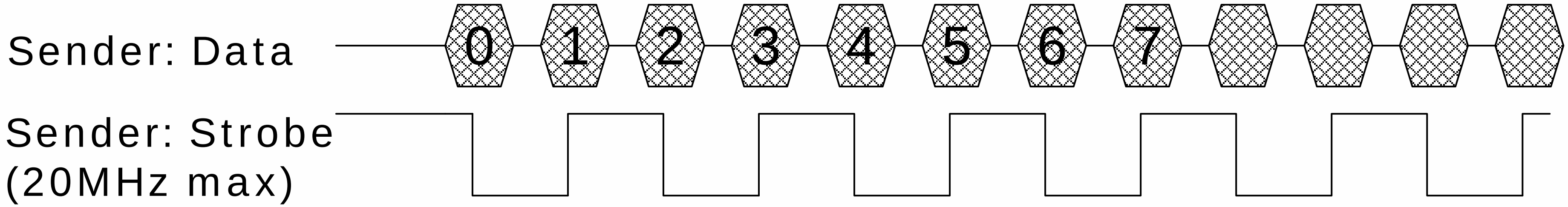
Full Handshake Protocol



2eSST Protocol



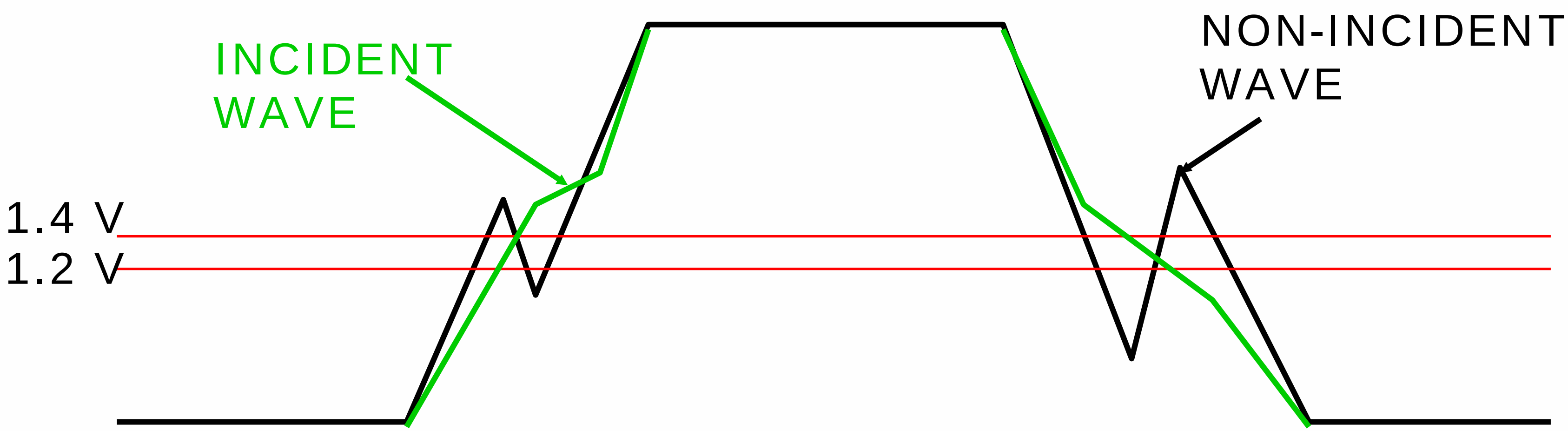
Benefits of 2eSST

- Practical data bandwidth of 320 MBps.
- Broadcast capable to multiple slaves in one transfer
- Products are backward compatible with existing products:
  - Capable of communicating at both 2eSST speeds and at regular VMEbus speeds.
  - Existing products communicate using existing VMEbus protocols.
  - Mix and match on the same bus – talk at fastest speed possible.
  - Protects investments.
- All this in existing VMEbus systems.
  - Stay in your existing chassis.
  - Protect your investment.

Other Requirements

- 2eSST operation requires new transceivers that support incident wave switching:
  - Once the edge crosses the threshold it must not bounce back in spite of reflections from the edge of the backplane.
- Texas Instruments has developed these new transceivers :
  - Announced April, 2002.
- These new transceivers are backwards compatible and are supposed to work with existing VMEbus bridge chips.

Incident Wave Switching



- Non-incident wave: a valid signal level is achieved only after the signal has been reflected off the end of the backplane.
- Incident wave: a valid signal level is achieved on the first trip of the signal down the backplane.

General Information on TI's New Transceiver

- SN74VMEH22501 transceiver was announced by TI in April 2002
- Optimized for driving large capacitive loads with controlled edge rates
- Has tight input-switching thresholds of ½(Vcc) +/- 50 mV for increased noise immunity
- Utilizes a supply voltage (Vcc) of +3.3Vand has +5V tolerant inputs to allow operation under the standard VMEbus legacy termination scheme
- Full specifications, data sheets, device models, and sample requests are available through the TI website (http://www.ti.com).

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2eSST Performance on Standard VME Backplanes

- ❒ Successful implementation of the VME 2eSST protocol in standard (non-proprietary) backplanes is an important goal of the VME Renaissance
- ❒ Test results to date show Texas Instruments' new VMEbus transceiver can be used to successfully implement the 2eSST protocol on standard VME64x five-row backplanes.
- ❒ MCG worked closely with Texas Instruments in the first half of 2002 to test the transceiver in approximately 55 different board configurations on standard 21-slot backplanes
  - ❖ Two 21-slot test chassis were used
    - One with a 5-row backplane
    - One with a 3-row backplane
- ❒ See the article in the August 2002 issue of VMEbus Systems Magazine for more details

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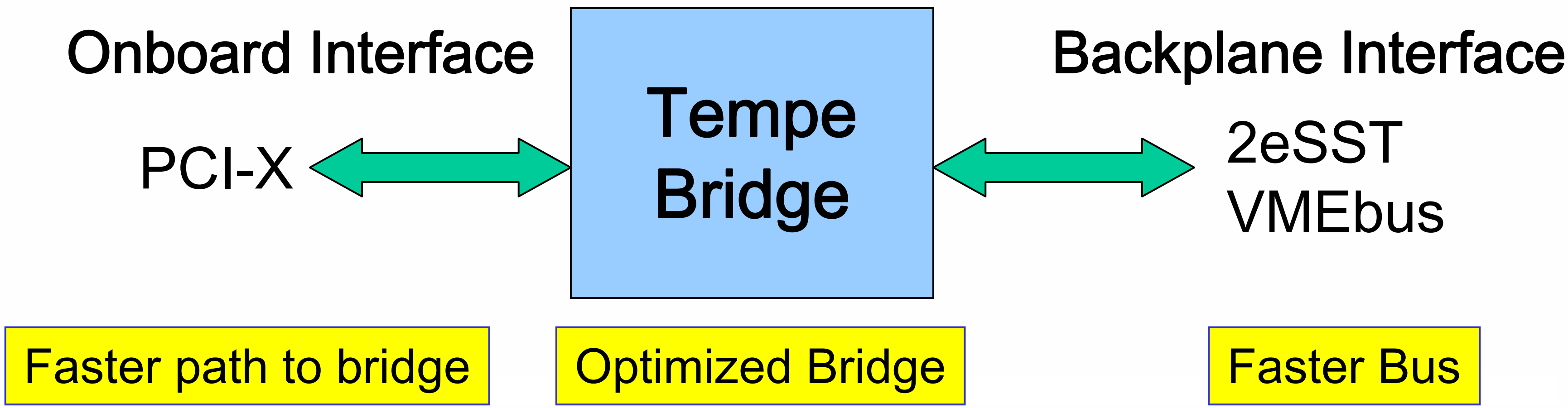
Conclusions Drawn From 2eSST Driver Testing

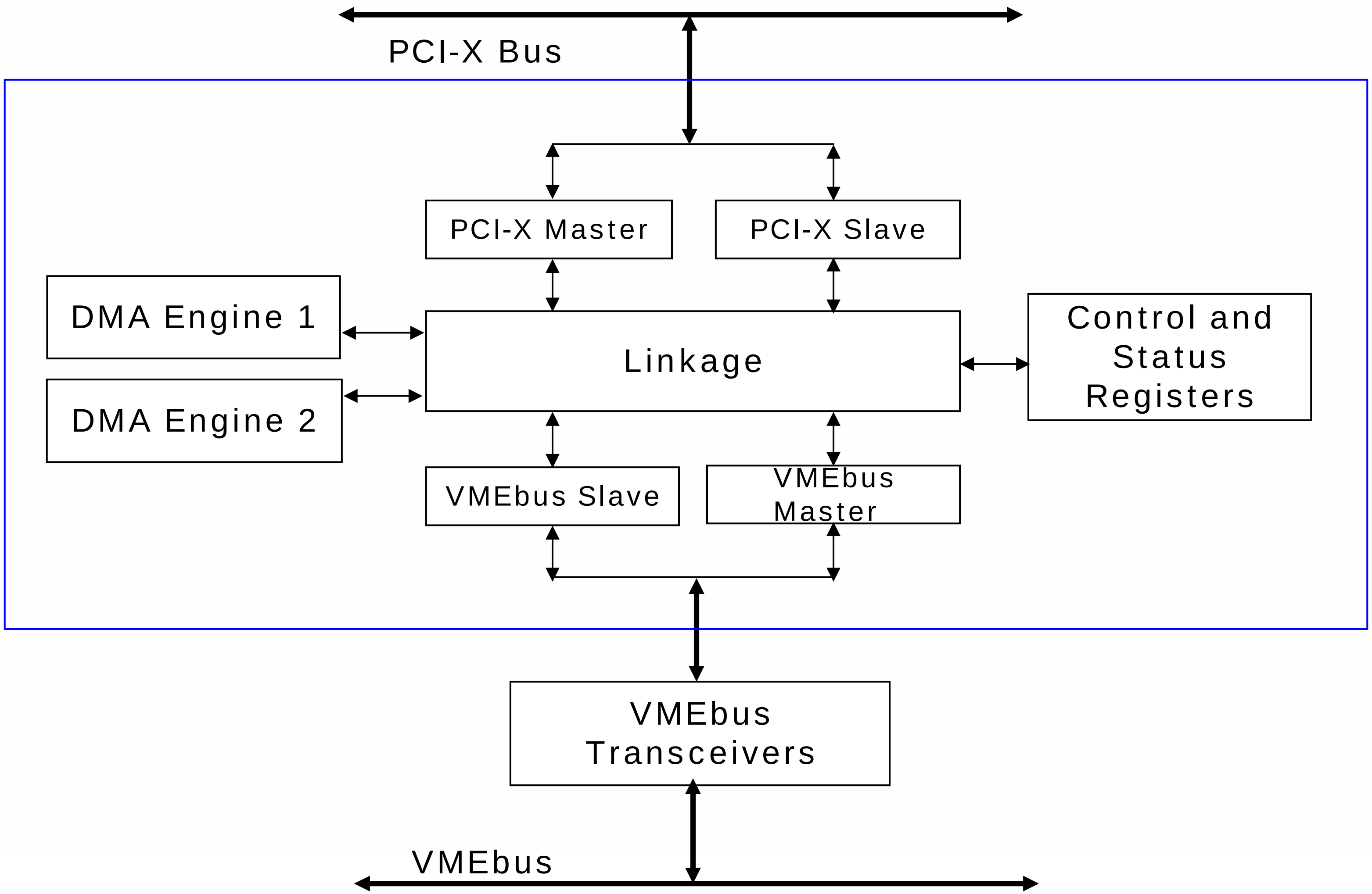
- The SN74VMEH22501 device performs reliably for standard VME64 transfers on a 3-row backplane
- A 5-row backplane is necessary for reliable VME 2eSST operation
- System margins can be maximized by
  - Adding AC return caps on 2eSST payload boards on Row D power pins
  - Distributing payload boards evenly in the chassis
  - Filtering VME control signal inputs
- The SN74VMEH22501 exhibits thermal characteristics similar to those of the SN74LVTH16245 (standard VMEbus drivers)

Tempe Bridge – an Advanced VMEbus ASIC

- Introduces the high-speed 2eSST protocol.
- Supports existing protocols:
  - Backwards compatibility with existing VMEbus protocols.
- Includes all other required VMEbus functions.
- PCI-X interface supports 33, 66, 100, 133 MHz operation.
- Includes two DMA engines.



Tempe Bridge Block Diagram



Tempe Features: VMEbus Master

- Supports A16, A24, A32 and A64 VMEbus addresses.
- Programmable AM codes.
- Supports D8 even, D8 odd, D16, and D32 transfers.
- Supports D16, D32 and D64 data widths for block transfers.
- Supports SCT, BLT, MBLT, 2eVME and 2eSST protocols.
- Supports RETRY during 2eSST transfers.
- Supports 2eSST broadcast.
- Programmable request level.
- Features not supported by the VMEbus Master:
  - A40 address modes.
  - D32 MBLT transfers.
  - VMEbus RETRY during SCT, BLT or MBLT transfers.

Tempe Features: VMEbus Slave

- Eight Programmable VMEbus map decoders.
- A16, A24, A32 and A64 addresses.
- 8-bit, 16-bit, and 32-bit single cycle data transfers.
- 8-bit, 16-bit, and 32-bit, and 64-bit block transfers.
- Supports SCT, BLT, MBLT, 2eVME and 2eSST protocols.
- Supports RETRY during 2eSST transfers.
- Supports 2eSST broadcast.
- 8 entry command and 4 Kbytes data write post buffer.
- 4 Kbytes read ahead buffer.
- Features not supported by the VMEbus Slave:
  - A40 address modes.
  - D32 MBLT transfers.
  - VMEbus RETRY during SCT, BLT or MBLT transfers.
  - VMEbus RMW cycles are not guaranteed indivisible on the PCI bus.

Tempe Features: VMEbus Utility

- VMEbus Interrupter.
  - Programmable IRQ1-IRQ7 request level.
  - Programmable 8-bit status/ID register.
  - Broadcast mode on IRQ1 (Non-VMEbus standard).
- VMEbus System Controller.
  - Always SCON, never SCON and auto SCON modes.
  - Arbiter modes.
    - Priority.
    - Round-robin.
    - Single-level.
    - Arbitration time out timer.
  - Programmable global time-out timer.
  - SYSRESET logic.
- Geographical Addressing.

Tempe Features: PCI Master

- Supports PCI-X enhancements.
- Supports 64-bit address.
- Supports 32 and 64-bit data transfers.
- Supports PCI MSI (Message Signaled Interrupts).
- Features not supported by the PCI-Slave interface:
  - PCI Lock signal.

Tempe Features: PCI Slave

- ❒ Supports PCI-X enhancements.
- ❒ Supports 64-bit address.
- ❒ Supports 32 and 64-bit data transfers.
- ❒ Eight programmable PCI map decoders.
- ❒ 8 entry command and 4 Kbytes data write post buffer.
- ❒ 4 Kbytes read ahead buffer.
- ❒ Features not supported by the PCI-Slave:
  - ❖ PCI Lock signal.

Tempe Features: DMA Controllers

- Two DMA engines.
- Supports all implemented transfers:
  - PCI-to-PCI.
  - VMEbus-to-PCI.
  - PCI-to-VMEbus.
  - VMEbus-to-VMEbus.
- 4096 byte buffer.
- DMAC command chaining through a single-linked list of commands.

Tempe Features: Other

- Global Control & Status Registers.
- 3.3V I/O power.
- 1.8V core power.
- TBD-pin BGA package.

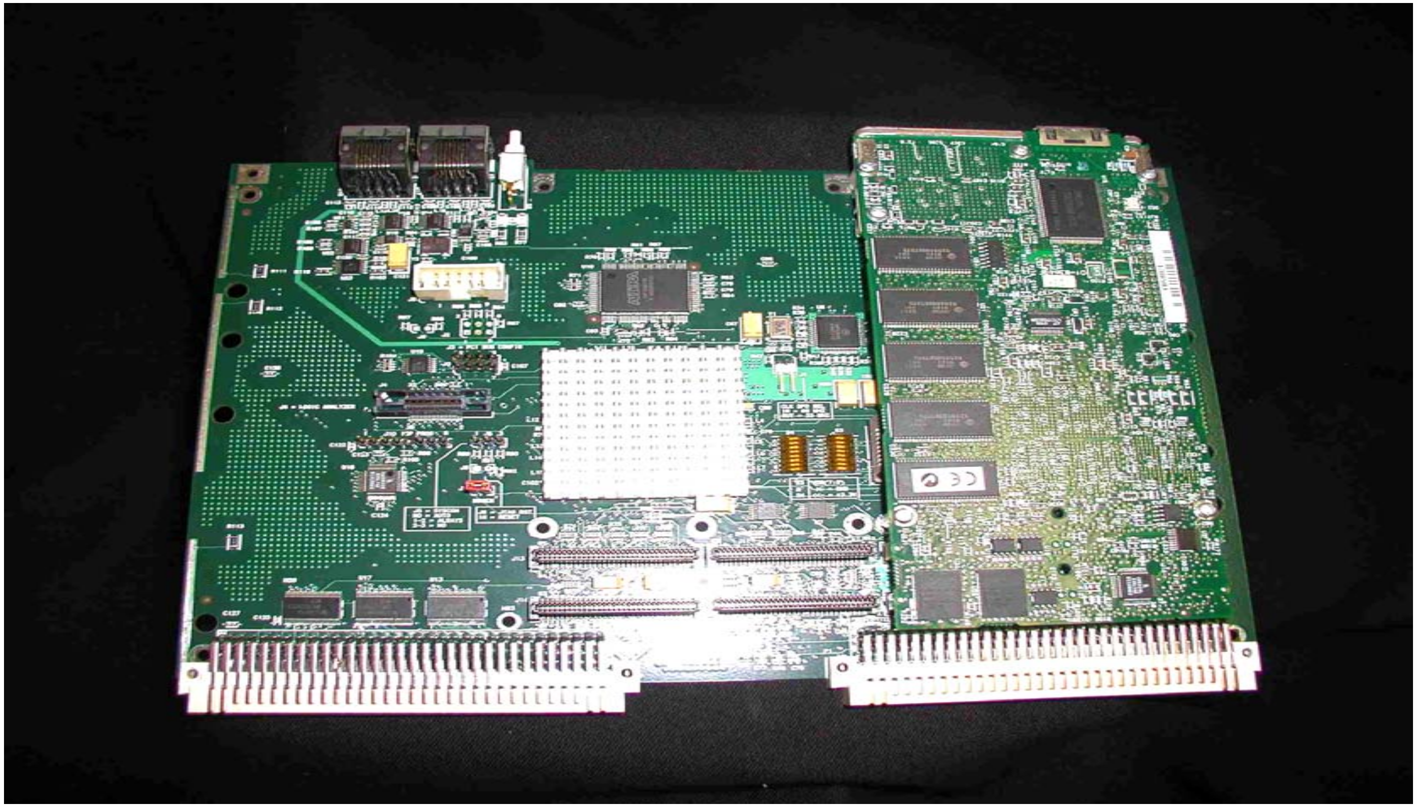
Tempe ASIC – Tundra Agreement

- Licensing and distribution agreement in place with Tundra
  - Press Release distributed on August 14
- Tundra will control production, marketing, sales, support, and early access program
- Tundra will have the ability to create re-spins and derivative products
- Tempe will be a Tundra product, not an MCG product
- All customers interested in Tempe should contact Tundra

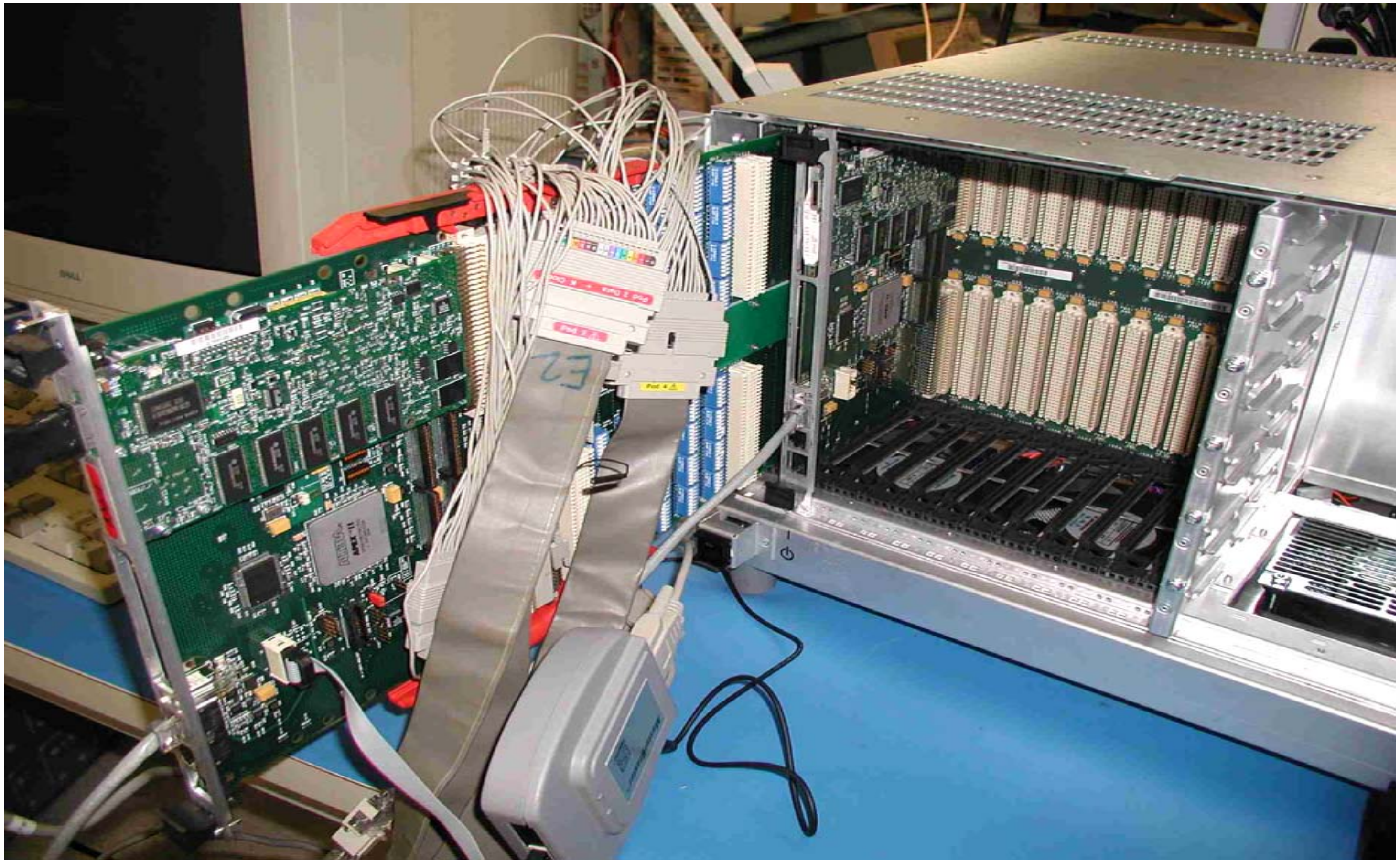
Tempe ASIC Development Status

- MCG Engineering has completed the design of the Tempe
- Tempe's logic is currently being tested using both simulation and actual POC (proof-of-concept) boards
- POC VMEbus boards include the new TI VMEbus transceivers and an FPGA that implements internal logic of the Tempe ASIC running at ¼ speed
  - A number POC boards are communicating with each other using the 2eSST protocol across a standard VMEbus backplane

Tempe ASIC POC Board



POC Boards Being Tested in a VME Chassis



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Enabling the 2eSST Market

- MCG will use the Tempe Bridge on new VMEbus designs.
- To accelerate the adoption of 2eSST, MCG has made the Tempe Bridge available to the VMEbus market through Tundra
- MCG will respin the chip as necessary.
- MCG will make available future VMEbus chips in a similar manner.

Tempe Bridge Benefits Summary

- ❒ Faster VMEbus (2eSST).
  - ❖ 8X current VMEbus.
- ❒ Host side interface (PCI-X).
  - ❖ Processor agnostic.
  - ❖ Faster than current offerings (PCI).
- ❒ Protects existing investment.
  - ❖ Application Software.
  - ❖ Boards.
  - ❖ Chassis & Backplane.
- ❒ Leverages and extends the VMEbus ecosystem.
- ❒ Tempe Bridge available to others.
- ❒ Future enhancements contemplated – not a point product.