Draft For Comment

SNS RF Timing System Requirements

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Background – Basic Timing Model

In the basic SNS timing model, a 60 (or 120) Hz reference source, phase locked to the 60 Hz line frequency, generates a "Cycle Start" event in the Timing Master IOC. The Cycle-Start event, along with other events generated by the timing master, is sent down the event link to any interested IOC. At the local IOC level, these events trigger one or more gate generator modules (called V124S modules), which apply the appropriate delays, widths, and repeat counts to generate local timing gates for the area served by that IOC. In principle, all timing gates could be controlled from the Cycle Start event.

The timing events generated by the Timing Master determine the timing gate's maximum repetition rate, as well as its minimum starting time (delay). For example, any timing gate derived from the SNS event, "Cycle Start", will have a maximum repetition rate of 60 Hz (the rep-rate of the Cycle-Start event), and a minimum delay of 0 (relative to the start of the machine cycle). Below is a list of the RF system timing requirements as we currently understand them:

General RF Timing System Requirements

- A given beam cycle may have one of 8 different identifying tags. This information is currently contained in the "User-ID" frame of the RTDL. This frame does not contain any specific beam characteristics (e.g. width of pulse, chopping pattern, etc.). It merely identifies one of 8 possible beam "flavors" and serves as an index into a set of tables maintained by the low-level RF control system to adaptively optimize performance for each beam type. One of the 8 user IDs is reserved for "No Beam".
- Separate timing gates are required for the klystrons and their power supplies. A single power supply may serve from one to twelve klystrons.
- The RF-specific timing gates all end at the same time in the machine cycle. This is the "Extract" time which occurs about 4.8 milliseconds after Cycle Start. Increasing the width of an RF-specific gate will cause it to grow backwards toward Cycle Start. Decreasing the width of an RF-specific gate will cause the starting point to move away from Cycle Start.

Linac RF Timing Requirements

The requirements for the Linac RF systems are as follows:

- To minimize power line harmonics and load fluctuations, all the power supplies should run at the same rep-rate. The power supply rep-rate should not change very frequently, and should be as evenly distributed as possible.
- The power supplies must turn on at least 100 microseconds before the Low-Level RF is gated on.
- In the cold linac, the Low-Level RF must turn on at least 300 microseconds before beam is turned on.
- In the warm linac, the Low-Level RF must turn on at least 100 microseconds before beam is turned on.
- In the warm linac, the Low-Level RF rep-rates and gate lengths, while constrained by their controlling power supply gates, may vary on a per-klystron basis.
- In the cold linac, the Low-Level RF rep-rates and gate lengths must be the same for every klystron in a given cryo-module.
- There is no need to run the RF above 60 Hz.
- The preferred failure mode for linac RF gates is "Always Off"

To meet these requirements, the SNS timing system will supply four events and four gates. The four events are:

- LinacHPRFEvent – Occurs about 3.4 milliseconds after Cycle Start. Determines the base rep-rate and maximum width for the High-Voltage power supply gates.

- LinacLLRFEvent – Occurs about 3.5 milliseconds after Cycle Start. Always occurs on the same machine cycle as the RFHV event. Determines the base rep-rate and maximum width for the Low-Level RF gates.
- LinacRFDiagEvent –Used to trigger diagnostic data acquisition. Occurs on demand (single-shot event). Although it is manually triggered, It is also "timed" to occur at any time during the machine cycle. It can also be "flavored" to occur on the same machine cycle as LinacLLRFEvent and on the same cycle as a specified User-ID. Timing is specified relative to LinacLLRFEvent (positive or negative).
- LinacRFEndEvent – Occurs at 60 Hz., slightly before T(Extract). Used to signal when the HPRF and LLRF gates should end.

The four gates are:

- LLRFPrePulse – Triggered in software by the LLRF IOC. Indicates that all required parameters have been written to the LLRF modules. Fixed width gate.
- HPRF – Generated by LinacHPRFEvent. Controls the RF High Voltage power supplies and RF Transmitters. Always ends at LinacRFEndEvent. Changing the gate width changes the starting time (relative to LinacHPRFEvent).
- LLRF – Generated by LinacLLRFEvent. Triggers the Low-Level RF. Always ends at LinacRFEndEvent. Changing the gate width changes the starting time (relative to LinacLLRFEvent).
- RFDiag – Generated by LinacRFDiagEvent. Triggers data acquisition for RF diagnostics. Fixed width gate.

The four gates are generated locally by V124S modules in the LLRF and HPRF IOC's. Normally, their lengths and rep-rates will be pre-determined by the Linac RF events listed above. For maintenance and conditioning purposes, however, provisions will be made for these gates to be independently controlled by the local IOC.

Implementation options:

- It may be desirable to have separate HPRF and LLRF events for the warm and the cold linac.
- To ensure consistency across all RF stands, the HPRF and LLRF gates may actually be generated by logic cards (V128 board from Brookhaven) rather than directly by the V124S modules.

Ion Source Timing Requirements

- To maximize the source stability and lifetime, the source RF should run at a constant rep-rate and a constant duty factor. This would typically be 60 Hz and one millisecond (6%) during production.
- Any modulation of the "beam gate" length and rep-rate will be implemented through the LEBT chopper.
- The source power supply gate will be independent of the rest of the RF system. When the accelerator is in "Standby" mode, the source gates will be shifted to be out of phase with the rest of the RF. This will insure that no beam is delivered past the RFQ while maintaining the thermal stability of both the source and the RFQ.
- The preferred failure mode for the source and RFQ RF gates is "Always On".

Implementation options:

- Unlike the rest of the RF, the ion source does not have separate high-power and low-level RF controls. Consequently there only needs to be a single event for controlling the source RF.
- The "Trigger Control Chassis" (part of the MPS) is responsible for determining whether the source RF gate should be in-synch or out-of-synch with the RFQ. This chassis is also responsible for turning of the low-level RF to the RFQ during latched fast-protect faults.