1 REAL TIME DATA LINK

The SNS Real Time Data Link (RTDL) is modeled after the RHIC Real Time Data Link [2]. It is a 10 Mhz, bi-phase mark encoded, differential PECL, serial link.

An *RTDL Frame* consists of 41 bits. Its payload is a 24 bit data word representing an SNS accelerator parameter pertaining to the upcoming machine cycle. The rest of the RTDL frame consists of a start bit, an 8-bit frame number, and 8-bit frame CRC. The format of an RTDL frame is:

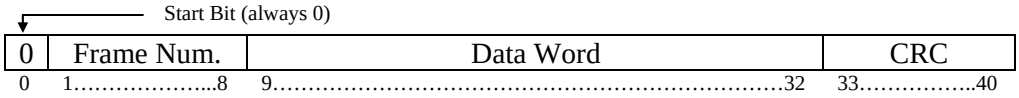

Figure 1
RTDL Frame Format

Before the start of each machine cycle, a series of frames about the upcoming cycle is transmitted on the RTDL. In the current SNS timing system, an RTDL transmission could contain up to 128 frames. 255 frames are possible if a third VME crate is added to the timing system. The last RTDL frame of the transmission is always frame 255 and contains a 24-bit "Message CRC" which is computed by the timing master IOC.

1.1 RTDL FRAME DEFINITIONS

These are the frames that currently constitute the RTDL transmission.

1.1.1 Time Stamp (Frames 1-3)

The first three RTDL frames contain the 64-bit EPICS timestamp to be applied at the next Cycle-Start event. The 64-bit timestamp is divided into two 32-bit long words as follows:

Seconds Past Epoch
Nanoseconds

Figure 2
EPICS Timestamp Format

The 64-bit EPICS timestamp is transmitted on three RTDL frames. The RTDL timestamp encoding is shown below:

RTDL Frame 1:	High-Order 24-bits of Seconds		
RTDL Frame 2:	MSB Nanoseconds	LSB Cycle Number	LSB Seconds
RTDL Frame 3:	Low-Order 24-bits of Nanoseconds		

Figure 3
RTDL Timestamp Format

The timing master IOC inserts the least significant byte of the current machine cycle number into the middle byte of the 2nd RTDL timestamp frame. This guarantees that each timestamp will be unique, even if the timing master IOC does not have an external clock source and is relying on the vxWorks clock for its system time (the vxWorks clock normally runs at 60 Hz and could return the same data for two consecutive cycles). This is important to the MPS system, which will fault if it detects that the RTDL timestamp is not changing (which it interprets to mean that

the timing master IOC is sick). Anyone else decoding the RTDL timestamp should disregard the middle byte of RTDL frame 2.

1.1.2 Ring Revolution Period (Frame 4)

RTDL frame 4 contains the ring revolution period in picoseconds. This value is useful for converting timing system units into real time. The ring revolution period is acquired my measuring the frequency of the event link clock. This process is described in section **Error! Reference source not found.**.

1.1.3 MPS Mode (Frame 5)

The MPS Mode number is broadcast on RTDL frame 5. This frame is primarily of interest to the MPS system. MPS uses the value in this frame to set the masks of which conditions to ignore and which conditions are relevant for the current operating mode.

The MPS system wants to make sure that the mode information coming from the RTDL is correct and does not contain any transmission errors. For this reason, the mode information is encoded three ways in RTDL frame 5. The low order byte contains the unadulterated mode number. The middle byte contains the mode times two plus one. The high order byte contains the "ones compliment" of the mode. This encoding is show below in Figure 4:

One's Compliment of Mode	(Mode × 2) + 1	Mode

Figure 4
RTDL Mode Frame Format

1.1.4 60 Hz. Phase Error (Frame 6)

This frame represents the distance in nanoseconds between the actual 60 Hz line frequency zero crossing and the "smoothed" zero crossing signal from the master reference generator (see section **Error! Reference source not found.**). This value is read from the master reference generator every cycle. It can be used to veto pulses or raise MPS conditions if the phase error gets outside the acceptable tolerance.

1.1.5 Beam Width (Frame 7)

This frame represents the width in turns of the current beam flavor. It is mainly used to synchronize diagnostic gates. If beam is scheduled to be on in the next cycle, this frame reflects the width of the particular flavor of beam scheduled for that cycle. If beam is off, this frame reflects the width of the primary flavor.

1.1.6 IOC Reset (Frame 15)

Each SNS Utility Module has a 24-bit "IOC Reset" address associated with it. This address is set by jumpers on the utility module board. When the utility module firmware detects a value in RTDL frame 15 that matches its own IOC Reset address, it will assert the VME SYSRESET line, causing the IOC to reboot. This feature allows an IOC to be rebooted remotely, even if its software is completely hung up. It will not, of course, allow for the remote reboot of a powered-off IOC.

IOC reboots are requested by writing the reset address of the specified IOC to a special record maintained by the RTDL encoder (V105S) driver. The record writes the IOC reset address

to a vxWorks *Message Queue*, which was also created by the RTDL encoder driver. Each cycle, the timing master sequencer reads this message queue, and if the queue is not empty, the next value is placed in RTDL frame 15.

RTDL frame 15 is broadcast every cycle (as are all the RTDL frames defined here). Normally its value will be 0, indicating that no IOCs should be rebooted.

1.1.7 Pulse Flavor (Frame 17)

RTDL frame 17 contains the "pulse flavor" of the next cycle. Pulse flavors are described in section **Error! Reference source not found.**.

1.1.8 RF Gate Widths (Frames 18-21)

The widths of the primary RF gates are broadcast in RTDL frames 18 through 21. These values can be used by the low-level and high-power RF IOCs to synchronize their local timing gates with the gate width values set in the timing master EDM screen. The assignments for the four RF gate width frames are shown below:

RTDL Frame 18:	Warm Linac High-Power RF Gate Width (turns)
RTDL Frame 19:	Warm Linac Low-Level RF Gate Width (turns)
RDTL Frame 20:	Cold Linac High-Power RF Gate Width (turns)
RTDL Frame 21:	Cold Linac Low-Level RF Gate Width (turns)

Figure 5
RF Gate Width Frames

1.1.9 Last Cycle Veto (Frame 24)

RTDL Frame 24 describes possible veto conditions to the experimental stations. Unlike the other RTDL frames, this frame pertains to the ***previous*** cycle rather then the ***next*** cycle. Each bit in this frame describes a reason why one or more experimental stations may want to veto data from the previous cycle. These bits are defined in the **snsTiming.h** file. 12 veto bits are currently defined. Their values and symbolic names are listed below:

Bit	Name	Description
0	VETO_NO_BEAM	No beam was delivered on the previous pulse.
1	VETO_NOT_TARGET_1	Beam was delivered to target 2 (not to target 1)
2	VETO_NOT_TARGET_2	Beam was delivered to target 1 (not to target 2)
3	VETO_DIAGNOSTIC_PULSE	Beam was a "reduced intensity" diagnostic pulse
4	VETO_PHYSICS_PULSE_1	Beam was one of the special physics study pulses
5	VETO_PHYSICS_PULSE_2	Beam was one of the special physics study pulses (the other type)
6	VETO_MPS_AUTO_RESET	Beam was interrupted by an "Auto Reset" MPS trip (fast protect)
7	VETO_MPS_FAULT	Beam was interrupted or not delivered because of a "Latched" MPS trip
8	VETO_EVENT_LINK_ERROR	Timing system detected corruption on the event link
9	VETO_RING_RF_SYNCH	Timing system has lost synch with the Ring RF signal
10	VETO_RING_RF_FREQ	Measured ring RF frequency is outside acceptable range
11	VETO_60_HZ_ERROR	60 Hz line phase error is out of tolerance

Figure 6
Veto Bit Definitions

1.1.10 Cycle Number (Frame 25)

The cycle number within the *Super Cycle* is broadcast on RTDL frame 25. An SNS super cycle is 600 cycles long. Therefore, this number will always be between 0 and 255. This information is useful for client IOCs that implement local rep-rates.

1.1.11 Message CRC (Frame 255)

The last RTDL frame transmitted is always frame 255. This frame contains a 24-bit CRC of the entire RDTL transmission. The CRC value is computed by the timing master. Details of the CRC computation can be found in [7