SNS UTILITY MODULE (V108S) FUNCTIONAL DESCRIPTION

Rev C.00

Rev C.00 – 21mar03 – updated I/O jumper list for Rev C boards, sec 4.8; added sec 4.17, 4.18
Rev B.01 – 1jul02 -updated remote reset jumper list, sec. 4.12
Rev B.00 – supports new features added for SNS utility module Rev B

Contents

Tables

Acronyms

A/D	Analog to Digital
CRC	Cyclic Redundancy Check
FIFO	First-In, First-Out
I&C	Instrumentation and Control
IOC	Input/Output Controller
LSB	Least Significant Byte
MSB	Most Significant Byte
OPTO	Opto-isolator
RORA	Release On Register Access
RTDL	Real Time Data Link
SNS	Spallation Neutron Source
VME	Versa Module Eurocard
VXI	VME Extensions for Instrumentation

1.0 INTRODUCTION

The following modifications were incorporated into the SNS utility module for Rev C:

1. Added pull-up resistors to support in-circuit JTAG programming of Altera chips.
2. Changed I/O connector configuration jumpers from solder jumpers to 0.1" header post jumpers that use standard shorting shunts.

The following modifications were incorporated into the SNS utility module for Rev B:

3. Addition of RTDL transmission valid and frame update bits.
4. Changed the operation of event link circuit such that multiple queued events can be read from the FIFO after the initial event that causes an interrupt and the FIFO has been changed to a single16 deep FIFO with no priority setting.
5. Added 2 output bits, toggled in software, 1 bit will drive an MPS opto input, the other bit can drive an opto or drive a 50 ohm signal (jumper selectable).
6. The 2 input bits were redesigned to be general-purpose inputs or configured to generate interrupts on rising/falling edge of an input signal. The 2 inputs can be driven from a 50-ohm source or 24-volt source (jumper selectable).

2.0 OVERVIEW

The SNS utility module (also known as a V108S) is a multi-purpose circuit board used to provide an Input/Output Controller (IOC) with interfaces to certain SNS communication links, input/output capability, and chassis environment information. The utility module, designed to reside in a VME chassis, occupies one VME board slot (4HP front panel width) and fits into a 6U X 160mm standard Eurocard form factor. The SNS utility module is also capable of being used in a VME Extensions for Instrumentation (VXI) chassis and in a VME-64X chassis. The utility module utilizes a 160-pin DIN male connector (P1 and P2) that is physically compatible with both the VME/VXI standard 96-pin DIN backplane connector as well as the VME-64X 160-pin DIN backplane connector. Note that the utility module does not use the new P0 connector specified for VME-64X. The front panel of the utility module contains connectors for input signals and LEDs to indicate certain status conditions. The 2 input bits and 2 output bits added for Rev B have P2 connections in addition to the front panel connections. These connections have jumpers so they can be disconnected from P2, yet maintain compatibility with VXI chassis. In addition, the Fan Fail signal has a P2 connection that can be disconnected with jumpers. When used in a VXI chassis, the SNS utility module requires a VME-VXI adapter or bus extender. The utility module requires +5V, +/-12V power. It also requires +3.3V when used in a VME64X chassis. The utility module communicates with the IOC over the VME backplane. The utility module's VME interface is a bus slave type and supports A24 addressing and D16, D8(o) and some limited D8(e) data transfers. D8(o) means odd byte transfers, D8(e) means even byte. The interrupter sections are I(x) interrupters, D8(o) and respond with an eight bit status/id on D00-D07. The interrupters on the utility module will clear interrupt requests using the Release On Register Access (RORA) method.

3.0 MAIN FEATURES

The following is a list of the main features and functions of the SNS utility module:

- SNS event link decoder and event link filter used to generate VME interrupts.
- SNS RTDL link receiver and data frame buffer.
- RTDL link error monitor, valid transmission status and frame update bits.
- Event link error monitor.
- Status indication for event link, SNS utility link and board initialization.
- Power supply, fan and temperature monitoring for the VME chassis.
- Interrupt generation from failed links, power supplies, fans and over temperature.
- Remote reset of VME chassis via the RTDL link.
- Two external input sources can be read or generate VME interrupts.
- Two output bits, 1 to drive the MPS system, the other is general purpose
- Board ID Prom.

4.0 DETAILED DESCRIPTION

4.1 VME Base Address of the Utility Module

The utility module will respond to A24 type addressing and to an address modifier code of 3D, standard supervisory data access (24 bit address) and 39, standard non-privileged data access (24 bit address). The base address of the utility module will be set using VME address bits A23-A14 and shall be user-selectable using jumpers provided on the utility module. For the purpose of providing the utility module's memory map and specific register examples, this document will assume a base address of 0xf0004000.

4.2 SNS Event Link Decoder Section

This portion of the utility module is responsible for receiving SNS event links and generating VME interrupts for those events specified by the IOC. This section will contain an event link receiver, filter lookup RAM and priority First In, First Out (FIFO). There are 256 unique event codes on the SNS event link. For each event there will be an associated entry in the filter RAM. Each entry will consist of an interrupt enable bit. The interrupt enable control bit is used to specify if the corresponding event link will be used to generate an interrupt or not. There is one vector register for all event links. The event link interrupt status-register read during the RORA interrupt acknowledge cycle will provide a read back of the event link that generated the interrupt. The following table summarizes the action of the control bit.

Interrupt Enable Ctrl Bit	Action
1	Event generates interrupt
0	Event does not generate interrupt

Table 4-1. Filter RAM Control Bits.

When the utility module receives an event link, its eight-bit code is used to address the filter RAM. If the interrupt enable bit is a 0 (zero) then no further action is taken. If the interrupt enable bit is a 1 (one)

and there are no other events pending, then an interrupt will be generated immediately. If there are other events pending, the event code will be queued in the FIFO. These queued events will not generate an interrupt, but must be flushed out of the FIFO by being read from the software. It is important to note that an event can only generate a VME interrupt after the FIFO has been completely emptied, thus the software must continue to check the empty status of the FIFO and must continue to read the FIFO until the status indicates empty. The next interrupt event to occur once the FIFO has been emptied will generate the next VME interrupt.

Note the difference between how SNS utility boards Rev B handle events compared to Rev A boards. For Rev A, each enabled event would generate a VME interrupt. For Rev B boards, only the initial enabled event queued into a completely empty FIFO will generate a VME interrupt. This change was implemented to reduce the number of event interrupts the IOC processor will have to handle.

The FIFO is 16 entries deep. If the FIFO is completely full, any new events are ignored and thus will be lost. A status byte indicating that a FIFO is full and events have been lost will be included. This status will be latched in a register, readable by the IOC over the VME bus. When read by the IOC, the status latch will be cleared.

It is important to note that caution should be used in the number of events used to generate interrupts for fast cycling machines. The FIFOs must be emptied by the end of a machine cycle. If a FIFO is not empty, then new events for the next cycle will not generate interrupts.

The utility module will assert only one VME interrupt line for all event links. The choice of a high priority/low priority event is strictly internal to the utility module. However, since there are seven VME interrupt lines, the utility module will provide a routing circuit that will allow the IOC to specify which one of the seven VME interrupt lines to use for event link interrupts. Table 4-2 summarizes the routing circuit control.

Table 4-2. Event Link Interrupt Routing Control

B2	B1	B0	Action
0	0	0	Disable VME interrupt
0	0	1	Route to VME interrupt Level 1
0	1	0	Route to VME interrupt Level 2
0	1	1	Route to VME interrupt Level 3
1	0	0	Route to VME interrupt Level 4
1	0	1	Route to VME interrupt Level 5
1	1	0	Route to VME interrupt Level 6
1	1	1	Route to VME interrupt Level 7

It will be the responsibility of the IOC to write the vector, the filter control bits and the routing control bits. Thus, these are available as readable/writable registers on the VME bus. The status/id returned during an interrupt service is the vector written into the event link interrupt vector register and will also be available on the VME bus. The following registers and memory locations are used for event link interrupt control and monitoring.

- Event link interrupt vector register - VME address 0xf0004065: This register contains the eight-bit status/id vector returned during an event link interrupt cycle. This register also supports standard VME D8(o) reads and writes.

- Event link interrupt routing register - VME address 0xf0004041: This register contains the VME interrupt level (1-7) for the event link interrupt. This supports standard VME D8(o) reads and writes. This register is eight bits wide with the following format, xxxxxB2B1B0, where x means don't care and B2, B1 and B0 are set as shown in Table 4-2 above. Note this register is reset to zero upon a VME system reset.

- Event link status register - VME address 0xf000405d: This register contains the hex code of the event link generating an interrupt and is read as a standard VME D8(o) read cycle by the interrupt handler routine. When this register is read, it will clear the interrupt request (RORA). This register is eight bits wide.

- FIFO status - VME address 0xf0004055: This register reads back different status conditions for the FIFOs. There are three conditions for the FIFO, full error, full and empty. Full error indicates that a write was attempted when the FIFO was already full. Full indicates that the maximum number of entries has been reached and empty indicates there are no entries in the FIFO. Full error status is active high, full and empty statuses are active low. After this register is read, only the full error status bits are cleared. This register supports VME D8(o) reads only. This register is eight bits wide and uses the following format, 00EF000Ferr, where:

  E = empty status for the FIFO, bit 5
  F = full status for the FIFO, bit 4
  Ferr = full error status for the FIFO, bit 0

- FIFO reset - VME address 0xf000406d: A read of this register is used to clear the FIFOs. This is important during initialization of the board. No valid information is returned when this register is read. Supports VME D8(o) reads only.

- Eventlink parity errors - VME address 0xf0005851: This register is a read back of event link parity errors. The read back is a two digit hexadecimal number. Errors are counted using an eight bit binary counter. The range of values is 00 - 255 decimal. The register is eight bits wide and supports VME D8(o) reads only.
- SNS event link frame errors - VME address 0xf000584d: This register is a read back of event link frame errors. The read back is a two digit hexadecimal number. Errors are counted using an eight bit binary counter. The range of values is 00 - 255 decimal. The register is eight bits wide and supports VME D8(o) reads only.

- Filter control - VME addresses 0xf0004801 - 0xf00049ff inclusive and odd addresses only: There are 256 of these locations, one for each event link. Each location uses the lower bit for the interrupt control using the following format 0000000I, where I is the interrupt enable control bit. Please refer to Table 4-1 above. To calculate which location corresponds to a particular event link, use the following formula: (event code in hex X 2) + 4801h. For example, use the following to find out the location for event 0Ah: (0Ah X 2) + 4801h = 4815h. Thus the location for this event is 0xf0004815. Each filter control location is eight bits wide and supports VME D8(o) reads and writes.

The following steps must be taken to insure proper initialization of the event link interrupt control at power up since the filter RAM will power up in a random state. This random state will cause false interrupts to occur if not properly initialized.

1. Clear the interrupt level by writing 00h to the event link interrupt routing register (0xf0004041).
2. Clear all filter control locations by writing 00h to each location, (0xf0004801-0xf00049ff).
3. Reset the FIFOs by reading the FIFO reset location (0xf000406d).
4. Clear any pending interrupts by reading the event link status register (0xf000405d).

The event link interrupt control is now initialized. To start interrupts do the following:

1. Write the desired event link interrupt vector to the vector register (0xf0004065)
2. Write the filter control bits to the desired filter locations.
3. Write the desired interrupt level to the routing register (0xf0004041)

4.3 SNS Real Time Data Link (RTDL) Receiver Section

This section of the utility board is responsible for receiving SNS RTDL link frames, storing them and making them available to the IOC. This section of the utility board consists of a receiver and a RAM frame buffer. The frame buffer will be 24 bits wide since each machine parameter consists of 24 bits of data. There are 256 different machine parameters and each will have its own entry in the buffer RAM. When a frame is received, its eight-bit parameter ID will be used as the address into the frame buffer RAM to write the data. RTDL link frames are transmitted on every machine cycle. A RTDL link frame actually consists of 41 bits. One start bit, eight bits parameter ID, 24 bits of data and an eight bit Cyclic Redundancy Check (CRC) checksum. The CRC checksum is used to insure the integrity of the ID and data bits and is not available to the IOC. For Rev B/C boards there will be an additional 2 bits available to the IOC. One bit will indicate that a frame has been updated; the other bit will indicate if the frame is valid, i.e., no CRC error has occurred during transmission of the frame. There will a set of these bits for each possible parameter ID. These bits are set by the hardware but must initialized and reset to 00 by software. The following table summarizes the meaning of the bits:

Table 4-3. RTDL Frame Status Bits.

FrameValid (B1)	FrameUpdate (B0)	Meaning:
0	0	Reset condition, data is NOT valid or old
0	1	Frame has been received, data is NOT valid
1	1	Frame has been received, data IS VALID
1	0	N/A condition

The software must set the Frame Valid (B1) and Frame Update (B0) bits to 00 after a frame is read.

RTDL frames start at location 0xf0006000. Each frame occupies four bytes of memory but since each frame consists of 24 data bits, only the lower three bytes carry any meaningful information. There are 256 four-byte locations, one for each possible SNS RTDL parameter id. Thus the range of addresses for all 256 frames is 0xf0006000 - 0xf00063ff in four byte sections. The four bytes are arranged in standard VME format with byte 0 being the Most Significant Byte (MSB) and byte three the Least Significant Byte (LSB). For the SNS RTDL link frames byte 0 is undeclared, and byte one contains the upper eight bits of the 24-bit frame. Byte two contains the middle eight bits of the 24, and byte three contains the lower eight bits. The IOC can read each frame as either four eight-bit bytes or as two 16-bit words. When read as 16-bit words, the upper word contains bytes 0-1 and the lower word bytes 2-3. To calculate the base address of any SNS RTDL frame, use the following formula: (SNS RTDL frame parameter id in hex X 4) + 6000h. For example if we wanted to access the SNS RTDL frame whose parameter id is 10 (0Ah), then the formula yields: (0Ah X 4) + 6000h = 6028h, thus the base address for this frame is 0xf0006028. Byte one is located at base plus one (1) (0xf0006029), byte two at base plus two (2) (0xf000602a) and byte three at base plus three (3) (0xf000602b). Valid range of parameter ids is 0 – 255.

Memory locations for the RTDL frame status bits start at address 0xf0006400, also organized in 4-byte blocks. The entire range for all 256 frames is 0xf0006400 – 0xf00067ff. Byte 3 contains the actual status bit readbacks, bytes 0, 1 and 2 are don't care. Byte 3 has the following format: 000000B1B0, with B1 and B0 as defined above in Table 4-3. To calculate the address for the status bits of any SNS RTDL frame, use the following formula: (SNS RTDL frame parameter id in hex X 4) + 6403h. For example if we wanted to access the status bits for the frame id used in the above example (10d or 0Ah), then the formula yields: (0Ah X 4) + 6403h = 642bh, thus the address for byte 3 is 0xf000642b. Byte 3 supports standard VME D08 reads/writes.

SNS RTDL frames can be read and written by the IOC, however writing is a special case that is only to be used to initialize the SNS RTDL frame buffers to 000000h and to reset the RTDL frame status readback bits. Only 00h should be written to bytes 1, 2 and 3 of a RTDL frame. It is also important to note that using the SNS utility link frame buffer area as a regular scratchpad RAM area will not work. Writing data besides 0000h will result in unexpected and erroneous data.

4.4 SNS RTDL Transmission Error Count

A count of transmission errors from the SNS RTDL link will be recorded and available to the IOC. Transmission errors are counted in a 16-bit binary counter. The count value will indicate the number of detected errors. RTDL frames are transmitted with an eight-bit CRC checksum byte. As the frame is received, a CRC checksum on the incoming frame is calculated. The transmitted CRC checksum must match the computed CRC checksum in order for the frame to be valid. If they do not match, the SNS RTDL receiver will output a transmission error signal that will clock the error counter. The following registers are associated with the RTDL transmission error count.

- SNS RTDL transmission error count, high byte - VME address 0xf0004051: This register is the high byte read back of the SNS utility link transmission errors. This register is eight bits wide and supports VME D8(o) reads only.

- SNS RTDL transmission error count, low byte - VME address 0xf000404d: This register is the low byte read back of the SNS utility link transmission errors. This register is eight bits wide and supports VME D8(o) reads only.

4.5 Power Supply, Fan, Temperature and Links Monitor

This section of the utility module will monitor the +5V, +12V, -12V VME chassis DC power supplies, plus the +3.3V DC power supply for theVME64X chassis, the five chassis cooling fans (note: the five status signals for the fans are wired OR'ed and only one status bit is brought to the utility module), the chassis temperature and the event link and SNS RTDL link. Together these comprise an environment monitor. If any of these is found to be working improperly, the utility module will assert a VME interrupt. Note only one interrupt per fault, per condition will be generated. If a fault remains active, the utility module will not continuously generate interrupts for that fault. The fault must first go inactive before another interrupt is generated. Also each fault condition will be monitored independently they can each independently assert an interrupt. Status registers will be provided on the utility module that the IOC can read and will contain the information on exactly what has failed. As part of the system for monitoring a chassis, DC power supplies and digitized read backs of the power supply voltages will be available to the IOC. The utility module will digitize the +5V, +12V, -12V, +5V ripple, +3.3V and the +3.3V ripple. Each voltage read back will be available to the IOC as an eight bit quantity. Digitizing of the voltages will take place at a five Hz rate (every 200 mS). Note that any changes in the value of a digitized voltage read back will not generate a VME environment interrupt.

Note that the +3.3V read backs are only valid for theVME-64X chassis; there is no +3.3V in VXI or standard VME chassis. Also fans will not be monitored by the utility module in VXI chassis.

The microcontroller that monitors the environmental input status bits will not generate an interrupt until the environment vector register has been initialized. This will enable the proper handling of faults that might occur before the board has been initialized. This can occur, for instance, if the SNS utility link was disconnected while the chassis is being turned on. The following registers are used to control the environment monitor.

- Environment interrupt vector register - VME address 0xf0004049: This register contains the eight-bit status/id returned during an environment interrupt cycle. This register also supports standard VME D8(o) reads and writes.

- Environment interrupt routing register - VME address 0xf0004045: This register contains the VME interrupt level (1-7) for the environment interrupt. Supports standard VME D8(o) writes only. This register is eight bits wide with the following format, xxxxxB2B1B0, where x means don't care and B2, B1 and B0 are set as shown in the Table 4-4. Note this register is reset to zero upon a VME system reset.

Table 4-4 summarizes the routing circuit control for the environment interrupt.

Table 4-4. Environment Interrupt Routing Control Bits.

B2	B1	B0	Action
0	0	0	Disable VME interrupt
0	0	1	Route to VME interrupt Level 1
0	1	0	Route to VME interrupt Level 2
0	1	1	Route to VME interrupt Level 3
0	1	1	Route to VME interrupt Level 4
1	0	0	Route to VME interrupt Level 5
1	1	0	Route to VME interrupt Level 6
1	1	1	Route to VME interrupt Level 7

- Environment interrupt routing read back register - VME address 0xf0004041: This register is the read back for the environment interrupt level routing. This register supports VME D8 (o) reads and has the following format xB2B1B0xxxx where x is don't care and B2, B1 and B0 are as shown in the Table 4-4 above.

- Environment status register - VME address 0xf0004069: This register contains the status bits for the power supplies and the cooling fans and is read as a standard VME D8(o) read cycle by the interrupt handler routine. When this register is read, it will clear the interrupt request (RORA). This register is eight bits wide and has the following format: b7b6b5b4b3000, where 0 will be read as a logic 0 and the other bits have the following meaning:

  b7 = +5V status
  b6 = -12V status
  b5 = +12V status
  b4 = fan status (only valid for VME chassis)
  b3 = +3.3V status (only valid for VME-64X chassis)

  Each status bit indicates its respective fault condition with a logic one and normal operation (no fault) with a logic 0.

- Link status register - VME address 0xf0004059: This register contains the status bit for the temperature high read back and status bits for the various links. This register is eight bits wide and supports standard VME D8(o) reads. It has the following format: xxb5b4b3b2b1b0, where x means don't care and the rest of the bits have the following meaning:

  b5 = remote reset routing, (1) remote reset drives VME /SYSRST, (0) reset drives P2 connector pin
  b4 = temperature high status, indicates over temperature fault has occurred
  b3 = board initialization bit
  b2 = board configuration, (0) configured for VME, (1) configured for VXI
  b1 = event link status
  b0 = SNS RTDL link status

The initialization bit (b3) will indicate that the software has initialized the board. This bit is cleared by a VME system reset and will read logic '0' when the board has been reset and not yet initialized. The bit will be set to logic '1' when the event link FIFO reset register (0xf000406d) is read.

The configuration bit (b2) will indicate if the utility module is configured for VME which means the connections to P2 can be used, or configured for VXI, which means the P2 connections, cannot be used.

The temperature high status/link status is part of the environment monitor system that can generate VME interrupts. Thus this register must also be read as part of the environment interrupt handler, however reading this register does not clear an interrupt request. To properly acknowledge an environmental interrupt, both the link status and the environment status register must be read as part of the interrupt handler.

The temperature high status bit reads logic one when an over temperature fault has occurred. The link status bits read logic one when a carrier signal is detected on each respective link and thus a logic one read back indicates normal operation for that link. A read back of logic 0 indicates no carrier has been detected and thus the link is not operational.

The over temperature threshold will be preset for 55 deg. C since most of the semiconductor components used on various boards have an operating temperature limit of 70 deg. C.

- Temperature read back register - VME address 0xf0004061: This register contains the actual temperature read back from the temperature sensor. It is eight bits wide and supports standard VME D8(o) reads only. To convert the reading to Celsius, simply divide the reading by two. For example using a read back of 0x3C, this would be 60 in decimal form. 60/2 = 30, thus the temperature is 30 deg. C. A temperature reading is taken once every five seconds.

- Temperature High Limit Set Point register – VME address 0xf0005869: This register contains the high limit or over temperature threshold setting for the temperature sensor. The utility module driver should initialize this value to 55 deg C. This register is eight bits wide and supports standard VME D8 (o) reads and writes. To set the over temperature threshold, simply write the desired value to this register. For example to set a threshold of 62 deg C, write 62d (0x3E) to the register. The on board microcontroller will detect the new set point and update the temperature sensor. Valid range is +20 deg C to +120 deg C.

- +5V A/D read back register - VME address 0xf0004087: This register is the +5V read back. It is eight bits wide and supports VME D8(o) only. The value in the register is an eight bit hexadecimal number. To convert to an actual voltage value, use the following formula where rdbkval is the value obtained from reading this register: (((rdbkval * 4.096)/256) * 2) = volts. For example, a reading of 0x9A = 154d. Then plugging in this value yields: ((154*4.096)/256) * 2 = +4.92V.

- +3.3V A/D read back register - VME address 0xf0004089: This register is the +3.3V read back. This value is only valid in VME64X chassis, which provide +3.3V on the back plane. It is eight bits wide and supports VME D8(o) only. The value in the register is an eight bit

hexadecimal number. To convert to an actual voltage value use the following formula where rdbkval is the value obtained from reading this register: ((rdbkval * 4.096)/256) = volts. For example a reading of 0xCD = 205d. Then plugging in this value yields: ((205*4.096)/256) = +3.28V.

- +12V A/D read back register - VME address 0xf000408B: This register is the +12V read back. It is 8 bits wide and supports VME D8(o) only. The value in the register is an eight bit hexadecimal number. To convert to an actual voltage value, use the following formula where rdbkval is the value obtained from reading this register: (((rdbkval * 4.096)/256) * 3) = volts. For example, a reading of 0xF9 = 249d. Then plugging in this value yields: ((249*4.096)/256) * 3 = +11.95V.

- -12V A/D read back register - VME address 0xf000408D: This register is the –12V read back. It is eight bits wide and supports VME D8(o) only. The value in the register is an eight bit hexadecimal number. To convert to an actual voltage value, use the following formula where rdbkval is the value obtained from reading this register: (((rdbkval * 4.096)/256) * 3) = -volts. For this reading, the negative of the result is required. For example, a reading of 0xF8 = 248d. Then plugging in this value yields: ((248*4.096)/256) * 3 = 11.79V, then negate yielding –11.79V.

- +5V ripple A/D read back register - VME address 0xf000408F: This register is the +5V ripple read back. It is eight bits wide and supports VME D8(o) only. The value in the register is an eight bit hexadecimal number. To convert to an actual voltage value, use the following formula where rdbkval is the value obtained from reading this register: (((rdbkval * 4.096)/256)/20) = volts. For example a reading of 0x51 = 81d. Then plugging in this value yields: ((81*4.096)/256)/20 = +0.0648V = 64.8mV ripple on the +5V power supply.

- +3.3V ripple A/D read back register - VME address 0xf0004091: This register is the +3.3V ripple read back. This value is only valid in VME64X chassis, which provide +3.3V on the backplane. It is eight bits wide and supports VME D8(o) only. The value in the register is an eight bit hexadecimal number. To convert to an actual voltage value, use the following formula where rdbkval is the value obtained from reading this register: (((rdbkval * 4.096)/256)/20) = volts. For example a reading of 0x3C = 60d. Then plugging in this value yields: ((60*4.096)/256)/20 = +0.048V = 48mV ripple on the +3.3V power supply.

To initialize the environment interrupt control after power up, perform the following steps:

1. Write 0h to the environment routing register (0xf0004045)
2. Read the environment status register (0xf0004069). This clears interrupt requests.

Now to start valid interrupt generation upon an environmental fault, do the following:

1. Write the desired interrupt vector to the vector register (0xf0004049)
2. Write the desired interrupt level to the routing register (0xf0004045).

4.6 Remote Reset

The SNS RTDL link can provide remote reset capability for each IOC. Each VME chassis in the system will have its own unique remote reset address. The reset signal generated will be jumper selectable to drive either the VME /SYSRST line or P2A8. The signal to P2A8 can be disconnected with a jumper for compatibility with VXI. The jumper configuration selected is readable via the link status register (0xf0004059). Each remote reset address will be 24 bits in length and will be jumper selectable. An IOC can directly read the Remote Reset address from the utility module. The parameter ID for the reset frame will be fixed. When the remote reset circuit receives an address transmission, it will compare the received address to the chassis address. If the two are the same, the receiver will activate the VME system reset line (/SYSRST, pin C12 of the P1 connector) for approximately 225 mSec or pin P2A8. Note pin P2A8 contains its own pull up resistor. A remote reset address transmission will consist of one RTDL frame. Since the remote reset addresses are transmitted on the RTDL, protection against erroneous chassis resets are given by the CRC checksum transmitted with RTDL frames. There is no IOC support needed for the remote reset link other then to read the link status register (0xf0004059) to see if the remote reset link is active and where it is routed to. The following registers can be read from the utility module to get the 24-bit remote reset address. All are D8(o), read only.

- Remote Reset Code 1 (RCD1) - VME address 0xf0004081: This byte contains the upper eight bits of the remote reset address code.
- Remote Reset Code 2 (RCD2) - VME address 0xf0004083: This byte contains the middle eight bits of the remote reset address code.
- Remote Reset Code 3 (RCD3) - VME address 0xf0004085: This byte contains the lower eight bits of the remote reset address code.

4.7 Board ID Prom

The board ID prom will be readable by the IOC over the VME buss. It will contain the following information:

- Board type (i.e. this board is a utility module)
- Board serial number
- Version number

The address range for the ID prom is 0xf0004000 - 0xf000403f. Each information byte will support standard D8(o) VME reads. The even locations of the ID prom will be programmed with 2Eh. The 2Eh locations will support standard D8 (e) VME reads.

4.8 Input/Output Bits

The SNS utility module Rev B/C will provide 2 software settable output bits and 2 optically isolated input bits that can be used to generate interrupts.

Output 1 is dedicated to interface with the MPS system. It will drive a standard MPS opto-isolated input and also provides the MPS with a 2-wire loop-back used to test cable continuity. Output 2 is jumper selectable to drive either an opto-isolator input OR to drive a 50-ohm signal. Both outputs are independently set/reset from software. Jumper configuration is hardwired.

Both inputs are optically isolated and can be independently configured for 50-ohm TTL input or a 24V input such as a relay contact closure. Each input can also be independently configured to be read only or to generate a VME interrupt from an external signal source. Additionally if an input is configured to generate an interrupt, the rising or falling edge can be selected. Selection of 50-ohm/24V input sources is configured using hard-wired jumpers on the board. Selections of read-only/interrupt and rising/falling edge are software configurable options. Note: if both input channels are configured to generate interrupts, they use the same vector and interrupt level.

- Input Channel Configuration register - VME address 0xf0005841: This register contains the configuration control for the 2 input channels and the VME interrupt level (1-7) when external interrupts are used. Supports standard VME D8 (o) reads and writes. Note this register is reset to zero upon a VME system reset. (This register was the External interrupt routing register on Rev A SNS utility modules). This register is eight bits wide with the following format, xB6B5B4B3B2B1B0, x means don't care. B2, B1 and B0 set the interrupt level as shown in Table 4-5 below. B6, B5, B4 and B3 control Input 1 and 2's configuration as follows:

  B3 = Interrupt enable for Input 1, (1) - enable, (0) - disable
  B4 = Interrupt edge select for Input 1, (0) - rising edge, (1) - falling edge
  B5 = Interrupt enable for Input 2, (1) - enable, (0) - disable
  B6 = Interrupt edge select for Input 2, (0) - rising edge, (1) - falling edge

Table 4-5. Interrupt Routing Control Bits.

B2	B1	B0	Action
0	0	0	Disable VME interrupt
0	0	1	Route to VME interrupt Level 1
0	1	0	Route to VME interrupt Level 2
0	1	1	Route to VME interrupt Level 3
1	0	0	Route to VME interrupt Level 4
1	0	1	Route to VME interrupt Level 5
1	1	0	Route to VME interrupt Level 6
1	1	1	Route to VME interrupt Level 7

There is one vector register for both external interrupt sources. An external interrupt status register is read during the RORA interrupt acknowledge cycle and will provide a read back of which channel generated the interrupt. The frequency of the signal source generating external interrupt requests is limited by the response time of the IOC. Until the current interrupt is cleared during RORA, any new interrupt requests are ignored. The following registers are used for external interrupt control.

- External interrupt vector register - VME address 0xf0005865: This register contains the eight-bit status/id vector returned during an external interrupt cycle. This register also supports standard VME D8(o) reads and writes.

- External interrupt status register - VME address 0xf000585d: This register contains status bits that indicate which external interrupt channel generated the interrupt request. This register is read as a standard VME D8(o) read cycle by the interrupt handler routine. When this register is read, it will clear the interrupt request (RORA). This register is eight bits wide with the following format, xxxxxxC2C1, where x means don't care, C2 is the status bit for external interrupt from Input 2 and C1 is the status bit for external interrupt from Input 1. A one (1) indicates the channel is generating an interrupt request.

To turn on external interrupts do the following:

1. Read external int status register to clear int ff's, **very important for Rev B/C** (0xf000585d)
2. Write the desired vector to the external interrupt vector register (0xf0005865).
3. Write the desired interrupt level and control bits to the input channel configuration register (0xf0005841).

To turn off external interrupts do the following:

1. Write 00h to the external interrupt routing register (0xf0005841).

- Input/Output Bits register - VME address 0xf000586b: This register contains the 2 output bits and the readbacks for the 2 input bits. Supports standard VME D8 (o) reads/writes for the output bits and VME D8 (o) reads for the input bits. Note the output bits are reset to zero upon a VME system reset. This register has the format xxxxB3B2B1B0:

  B0 = Output bit 1, VME reads/writes
  B1 = Output bit 2, VME reads/writes
  B2 = Input bit 1, VME reads only
  B3 = Input bit 2, VME reads only

Jumper lists for the Input/Output channel configurations (SNS utility Rev C) are as follows. These jumpers are 0.1" header posts that use a standard 2 position shorting shunt (DigiKey part no. SSC02SYAN):

Input Channel 1

50 ohm input signal:	24V input signal:
[ ] JP16 IN	[ ] JP16 OUT
[ ] JP17 IN	[ ] JP17 OUT
[ ] JP18 IN	[ ] JP18 OUT
[ ] JP19 IN	[ ] JP19 OUT
[ ] JP20 OUT	[ ] JP20 IN
[ ] JP21 OUT	[ ] JP21 IN
[ ] JP22 OUT	[ ] JP22 IN
[ ] JP23 OUT	[ ] JP23 IN

Input Channel 2

50 ohm input signal:	24V input signal:
[ ] JP24 IN	[ ] JP24 OUT
[ ] JP25 IN	[ ] JP25 OUT
[ ] JP26 IN	[ ] JP26 OUT
[ ] JP27 IN	[ ] JP27 OUT
[ ] JP28 OUT	[ ] JP28 IN
[ ] JP29 OUT	[ ] JP29 IN
[ ] JP30 OUT	[ ] JP30 IN
[ ] JP31 OUT	[ ] JP31 IN

Output Channel 2

50 ohm drive:	Opto-isolator drive:
[ ] JP14 IN	[ ] JP14 OUT
[ ] JP15 OUT	[ ] JP15 IN

NOTE: see sec. 4.18 for I/O jumper list for SNS utility boards with serial numbers SN11 – SN50

4.9 SNS Utility Module Memory Map - Rev B/C boards

The Utility Module Memory Map in Table 4.6 shows all the memory locations described in the document above. This table assumes a board base address of 0xf0004000.

Table 4-6. Utility Module Memory Map.

Description	VME Address/Address Range
ID PROM	0xf0004000 – 0xf000403f
Event INT Routing/ENV. INT Routing Read Back	0xf0004041
Environment INT Routing	0xf0004045
Environment INT Vector	0xf0004049
SNS RTDL Xmit Error (lo byte)	0xf000404d
SNS RTDL Xmit Error (hi byte)	0xf0004051
Event Link FIFO Status	0xf0004055
Link Status	0xf0004059
Event Link Code Status	0xf000405d
Temperature Read Back Register	0xf0004061
Event Link Interrupt Vector	0xf0004065
Environment Status	0xf0004069
Event Link FIFO Reset	0xf000406d
Remote Reset Address Code 1 (hi byte)	0xf0004081
Remote Reset Address Code 2 (mid byte)	0xf0004083
Remote Reset Address Code 3 (lo byte)	0xf0004085
+5V A/D Read Back Register	0xf0004087
+3.3V A/D Read Back Register	0xf0004089
+12V A/D Read Back Register	0xf000408B
-12V A/D Read Back Register	0xf000408D
+5V Ripple Read Back Register	0xf000408F
+3.3V Ripple Read Back Register	0xf0004091
Event Link Filter control RAM	0xf0004801 – 0xf00049ff
Input Channel Configuration register	0xf0005841
Event Link Frame Errors	0xf000584d
Event Link Parity Errors	0xf0005851
External Interrupt Status	0xf000585d
External Interrupt Vector	0xf0005865
Temperature High Limit Set Point Register	0xf0005869
Input/Output Bits Register	0xf000586b
SNS RTDL Frame Buffer RAM	0xf0006000 – 0xf00063ff
SNS RTDL Frame Status Bits	0xf0006400 – 0xf00067ff

4.10 ID Prom Information

Displaying the ID prom from a typical utility board will provide the following information:

`*.V.M.E.I.D.S.N.S*:` This board manufactured by SNS
`*.V.1.0.8.S.....*:` Board type, V108S is the utility board identifier
`*...C.....0.0.2.7*:` Rev C, serial number 27
`*...U.T.I.L.I.T.Y*:` Utility module

4.11 Backplane Configuration

For SNS utility modules used in chassis' with non-active backplane configuration circuitry, the following P1 backplane jumper configuration is required for the slot that the board will be in:

Removed
[ ] BG0
[ ] BG1
[ ] BG2
[ ] BG3
[ ] IACK

A two-pin connector for the fan fail sensor is factory wired to the P2 connector of slot two, thus the utility board should be placed in this slot. However, the connector could be moved to slot three if needed. If the sensor connector is moved to slot three, the following connections must be made:

Blue wire to P2A5
Black wire to P2A6

4.12 Remote Reset Configuration Jumpers

To have the remote reset signal drive the VME /SYSRST line (P1-C12), the following jumper configuration must be used:

[ ] JP5 1 - 2
[ ] JP13 1 - 2

To have the remote reset signal drive P2-A8 (user defined), the following jumper configuration must be used. Please note this is valid for VME only, **for VXI this connection must not be used.**

[ ] JP5 2 - 3
[ ] JP13 2 - 3
[ ] JP4-1 IN

The **remote reset address jumpers** for each utility module are preconfigured and do not require any action by the user. The jumpers for the reset address are JP7-1 – JP7-24, inclusive. JP7-1 is the most significant bit of the 24-bit reset address; JP7-24 is the least significant bit. To set a reset address bit to logic 1, remove (out) the associated shorting jumper. To set a reset address bit to logic 0, insert (in) the associated shorting jumper. These jumpers use standard 0.1inch center, two position-shorting jumpers (shunts).

Example: a reset address of **0xADC053** would use the following starting with JP7-1:
out, in, out, in(A); **out, out, in, out**(D); **out, out, in, in**(C); **in, in, in, in**(0);
in, out, in, out(5); **in, in, out, out** 3)

4.13 VME/VXI Configuration

To configure the Utility Module for **VME** chassis, the following jumpers need to be **INSERTED**:

[ ] JP4-1 (aux remote reset) IN
[ ] JP4-2 (opto anode, Input 1) IN
[ ] JP4-3 (opto cathode, Input 1) IN
[ ] JP4-4 (opto anode, Input 2) IN
[ ] JP4-5 (opto cathode, Input 2) IN
[ ] JP4-6 (chassis fan fail signal) IN
[ ] JP4-7 (chassis fan fail ground) IN
[ ] JP4-8 (board configuration bit) IN

IN = insert shorting jumper

To configure the Utility Module for **VXI** chassis, the following jumpers must be **REMOVED**:

[ ] JP4-1 (aux remote reset) OUT
[ ] JP4-2 (opto anode, Input 1) OUT
[ ] JP4-3 (opto cathode, Input 1) OUT
[ ] JP4-4 (opto anode, Input 2) OUT
[ ] JP4-5 (opto cathode, Input 2) OUT
[ ] JP4-6 (chassis fan fail signal) OUT
[ ] JP4-7 (chassis fan fail ground) OUT
[ ] JP4-8 (board configuration bit) OUT

OUT = remove shorting jumper

All the above jumpers use standard 0.1-inch center, two position-shorting jumpers (shunts).

4.14 Front Panel Connectors and Indicators

- VME SEL – LED: lights when a utility module is being accessed from VME.
- UCRUN – LED: indicates that the environment monitor microcontroller is running. This LED blinks five times per second.
- EVENTLNK - LED and TWIN-AX connector: the TWIN-AX is used for Event Link input to the utility module. The LED will light when the utility module detects an active EVENT LINK carrier. The LED will be off when there is no active carrier.
- SNS RTDL link - LED and TWIN-AX connector: the TWIN-AX is used for SNS utility link input to the utility module. The LED will light when the utility module detects an active SNS utility link carrier. The LED will be off when there is no active carrier.

- I/O connector – 12 header will have the following pin assignments:
  pin 1 - drive for MPS HCPL 2612 opto isolator, output Chan 1
  pin 2 - MPS opto isolator return
  pin 3 - Short to pin 4 for MPS diagnostic
  pin 4 - Short to Pin 3 for MPS diagnostic
  pin 5 - drive for opto isolator or 50 ohm driver, jumper selectable, output Chan 2
  pin 6 - opto isolator return
  pin 7 - not used
  pin 8 - not used
  pin 9 - opto LED anode, jumper selectable to be 50 ohm TTL or 24 V, input Chan 1
  pin 10 - opto LED cathode, jumper selectable to be 50 ohm TTL or 24 V, input Chan 1
  pin 11 - opto LED anode, jumper selectable to be 50 ohm TTL or 24 V, input Chan 2
  pin 12 - opto LED cathode, jumper selectable to be 50 ohm TTL or 24 V, input Chan

4.15 P2 Connections

The following P2 pins duplicate front panel connections:

J1 (12 pin header) - External input signal, Chan 1 ----------> P2C29
External input signal, Chan 1 return ----> P2C30

J1 (12 pin header) - External input signal, Chan 2 ----------> P2C31
External input signal, Chan 2 return ----> P2C32

J5 (2 pin header JP6) - Fan Fail Signal ----> P2A5
Fan Fail Ground ----> P2A6

The following P2 pins are for other functions:

Aux reset signal ----> P2A8

These P2 connections can only be used in VME chassis. VXI defines use for these pins and they cannot be used on a utility module housed in a VXI chassis. All these signals will have jumpers so that they can be disconnected from P2 for use in a VXI chassis or connected to P2, if desired, for use in a VME chassis.
See section 4.13 above for VME/VXI jumper configurations.

4.16 Base Address Jumpers

Jumpers JP1-1 – JP1-10, inclusive are used for setting the base address of the utility module. The utility module uses VME address bit A23 – A14, inclusive for the base address. All of these jumpers use standard 0.1inch center, two position-shorting jumpers (shunts). The following example is the jumper configuration for a base address of 0x4000:

[ ] JP1-1 IN (A23)
[ ] JP1-2 IN (A22)
[ ] JP1-3 IN (A21)
[ ] JP1-4 IN (A20)
[ ] JP1-5 IN (A19)
[ ] JP1-6 IN (A18)
[ ] JP1-7 IN (A17)
[ ] JP1-8 IN (A16)
[ ] JP1-9 IN (A15)
[ ] JP1-10 OUT (A14)

IN = insert shorting jumper (logic 0)
OUT = remove shorting jumper (logic 1)
AXX = VME address bit AXX

4.17 Other Required Jumpers

The following are other jumpers that are needed for proper operation of the SNS utility module. All jumpers use standard 0.1inch center, two position-shorting jumpers (shunts).

[ ] JP10 IN
[ ] JP11 IN
[ ] JP12 IN

IN = insert shorting jumper

4.18 Special note for boards SN11 – SN50

SNS utility modules with serial numbers SN11 – SN 50, inclusive were originally Rev B boards that used 1206 size solder jumper pads for the I/O connector. Use the following jumper list for these boards (1206 size zero ohm resistors can be used):

Input Channel 1

50 ohm input signal:	24V input signal:
[ ] SJ1 IN	[ ] SJ1 OUT
[ ] SJ2 IN	[ ] SJ2 OUT
[ ] SJ3 IN	[ ] SJ3 OUT
[ ] SJ4 IN	[ ] SJ4 OUT
[ ] SJ5 OUT	[ ] SJ5 IN
[ ] SJ6 OUT	[ ] SJ6 IN
[ ] SJ7 OUT	[ ] SJ7 IN
[ ] SJ8 OUT	[ ] SJ8 IN

Input Channel 2

50 ohm input signal:	24V input signal:
[ ] SJ9 IN	[ ] SJ9 OUT
[ ] SJ10 IN	[ ] SJ10 OUT
[ ] SJ11 IN	[ ] SJ11 OUT
[ ] SJ12 IN	[ ] SJ12 OUT
[ ] SJ13 OUT	[ ] SJ13 IN
[ ] SJ14 OUT	[ ] SJ14 IN
[ ] SJ15 OUT	[ ] SJ15 IN
[ ] SJ16 OUT	[ ] SJ16 IN

Output Channel 2

50 ohm drive:	Opto-isolator drive:
[ ] SJ17 IN	[ ] SJ17 OUT
[ ] SJ18 OUT	[ ] SJ18 IN