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**PRELIMINARY**  
Specification for the  
V124S Trigger Module  
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## 1.0 Introduction

The SNS Event System consists of a centralized event encoder which operates from an RF clock that is 32X the ring revolution frequency, and distributed embedded decoders. The Trigger Module (V124S) is a general-purpose 6U x 4HP, VMEbus controlled module that is compatible with the SNS Event System and is designed to provide clocks and triggers for data acquisition systems and experiments.

This module provides eight identical channels that can be configured independently or in pairs, and a buffered recovered RF Clock output.

## 2.0 Configuration parameters

### **2.1 Board Configuration**

The following configuration parameters are programmable for the trigger module. These parameters are common to all channels. The associated hardware registers are listed for each parameter. See Section 5.3 for specific register definitions.

All delays are configured as a counter and a hold register. A VMEbus WRITE asynchronously (relative to the RF Clock) loads the hold register and the counter with the value on the VMEbus data lines. When enabled, the counter counts down to reach its terminal count (usually zero) and is synchronously loaded with the contents of the hold register depending on the configuration chosen. Both the counter contents and the hold register can be issued a VMEbus READ. Consecutive READs of the counter will yield different values if the counter is enabled to count.

#### **2.1.1 Command Register**

An eight bit register is provided to set the following parameters:

- a. Module Enable
- b. Ref/\*Auto

When all relevant parameters are configured, the module enable bit is set. This disables the OFFLINE Led on the front panel to signal that the module has been initialized. If the Event Link is inoperable, an option exists whereby a reference oscillator can be chosen as the link carrier clock. This function is for diagnostic purposes and always defaults to the link carrier clock.

#### **2.1.2 VME Interrupt configuration**

The trigger module generates a single VME Interrupt. Two eight bit registers are provided to configure the VME Interrupt level and interrupt vector. Any one of the following conditions can generate an interrupt:

- a. Timestamp source

- b. Timestamp Reset Event
- c. Event Link Carrier error
- d. Event Link Frame error
- e. Event Link Parity error
- f. Trigger Counter Terminal Count

### **2.1.3 RF Clock/Link Clock Delay**

An eight bit register is provided to allow a shift in the phase of the RF Clock/Link Clock output. RF Clock/Link Clock Delay is accomplished through an external (relative to all other delays) silicon delay line. An 8-bit value is loaded into the RF Clock/Link Clock Delay hold register and the RF Clock/Link Clock delay module. Resolution is 500ps. The delay is adjustable from 12ns (latency) to 139.5ns. (Input pulse width specifications need to be followed to realize the maximum delay.)

## **2.2 Channel Configuration**

Eight identical delay channels are provided. Each channel is configured with the following information:

### **2.2.1 Delay Control Register**

An eight bit register is provided to configure channel delay control data.

The following delay control is provided:

- Reload Counters on a Trigger Counter Terminal Count
- VMEbus Trigger Command
- VMEbus Reset Command - clears all counter and command values
- STOP - halts the RF clock to all counters
- Invert Output

### **2.2.2 Counter Control Register**

An eight bit register is provided to configure channel counter control data.

The following counter control data is provided:

- Revolution Delay Enable Select
- Sub-Revolution Delay Enable Select
- Trigger Counter Terminal Count Clock Select
- Pulse Width Counter Enable Select
- Fine Delay Clock Select

### **2.2.3 Revolution Delay Enable Selector**

The Revolution Delay Enable Selector allows the revolution delay counter to count each revolution clock. Counting will begin when set to one of the following configurations and after the occurrence of the appropriate trigger:

- a. VMEbus and Setting the VMEbus Trigger bit .
- b. Event and a decoded Event.
- c. External and external trigger input.
- d. Previous Channel Fine Delay Enable. (Not Channel 1.)

#### **2.2.4 Sub-Revolution Delay Enable Selector**

Sub-Revolution Counter Enable Selector allows the Sub-Revolution delay counter to count each  $1/(32 \cdot F_{rev})$  clock. Counting will begin when set to one of the following configurations and after the occurrence of the appropriate trigger:

- a. VMEbus and Setting the VMEbus Trigger bit.
- b. Event and a decoded Beam Synchronous Event.
- c. Revolution Delay Counter Enable/Revolution Delay Counter Terminal Count
- d. Revolution Delay Counter Terminal Count and its occurrence.

#### **2.2.5 Trigger Counter Clock Selector**

The Trigger Counter allows only a specified number of output triggers. The Trigger Counter will count occurrences of one of the following:

- a. Fine Delay Counter Clock.
- b. Next Channel Sub-Revolution Delay Counter Terminal Count.
- c. No clock .

#### **2.2.6 Pulse Width Counter Enable Selector**

Output Triggers can be configured for variable pulse widths in multiples of the  $1/(32 \cdot F_{rev})$  clock. The Pulse Width Counter is enabled by:

- a. Sub-Revolution Delay Counter Terminal Count

#### **2.2.7 Fine Delay Clock Selector**

Positioning of the output triggers within a Sub-Revolution is achieved by the Fine Delay Counter. The Fine Delay Counter Clock Selector is configurable to be the following:

Variable Pulse Width. One pulse from the Pulse Width Counter.

#### **2.2.8 Timestamp Configuration**

The Timestamp Counter can be configured to stop counting on the occurrence of one of the following:

- a. an Event .
- b. First Output Pulse (of a series).
- c. Trigger Counter Terminal Count .

### **2.2.9 Timestamp Clock Source**

The Timestamp Counter will count the occurrences of one of the following:

- a. The 29.5ns clock derived from the Event Link carrier frequency.
- b. an Event.

Details on the channel configuration parameters are provided in section 5.4.

## **2.3 On Board Memory**

VME ID Prom (64 bytes), Board Configuration registers (16 bytes), Channel Configuration registers (256 bytes), and Event Mask RAM (256 bytes) are mapped to VME A16 space on jumper selectable 2K byte boundary.

## **3.0 System Status parameters**

The following system configuration parameters are provided. These parameters are common to all 8-trigger channels. The associated hardware registers are listed for each parameter. See section 5.0 for specific register definitions.

### **3.1 Board Status**

#### **3.1.1 Interrupt/Error Status**

When a VME interrupt is generated by this module, the interrupt handler reads the interrupt status register to determine the cause of the interrupt. The error status register may be read outside the interrupt handler to determine the current status of the interrupt bits.

### **3.2 Channel Status**

#### **3.2.1 Status Flags**

Individual bits in this parameter field are used as status flags. The following status conditions are available:

#### WAITING\_FOR\_REV\_COUNTER\_ENABLE

This bit indicates that the Revolution Delay Counter has not been enabled.

#### WAITING\_FOR\_REV\_COUNTER

This bit indicates that the Revolution Delay Counter has been enabled but has not reached terminal count.

#### WAITING\_FOR\_SUB-REVOLUTION\_COUNTER\_ENABLE

This bit indicates that Sub-Revolution Delay Counter has not been enabled.

#### WAITING\_FOR\_SUB-REVOLUTION\_COUNTER

This bit indicates that Sub-Revolution Delay Counter Enable has occurred but the Sub-Revolution Delay Counter has not reached terminal count.

#### WAITING\_FOR\_TRIGGER\_COUNTER\_TERMINAL\_COUNT

This bit indicates that the Trigger Counter has not reached terminal count

#### RESET

This bit indicates that the channel is being held reset.

### 3.2.2 Revolution Delay

The Revolution Delay includes a 16-bit count-down counter that is loaded from the revolution delay hold register and counts the number of revolution clocks until terminal count is reached. This counter can count from 1 (945ns) to 65536 (61.97ms). It is enabled from the output of the Revolution Delay Enable Selector. The contents of the hold register are transferred to the counter on the occurrence of the Trigger Counter Terminal Count or Sub-Revolution Delay Enable. The following two values can be read via the VMEbus:

- a. Hold Register Value. This is the 16-bit value that is loaded into the Revolution Delay Counter.
- b. Current Count Value. This is 1sByte value of the Revolution Delay Counter. It is read on the fly and consecutive reads may yield different values. This value is used for diagnostic purposes.

### 3.2.3 Sub-Revolution Delay

The Sub-Revolution Delay includes a 8-bit count-down counter that is loaded from the Sub-Revolution Delay hold register and counts each occurrence of  $1/(32 * F_{rev})$ . This counter will allow a delay of more one revolution. It is enabled from the output of the Sub-Revolution Delay Enable Selector. The contents of the hold register are transferred to the counter on the occurrence of the Sub-Revolution Counter Terminal Count. The following two values can be read via the VMEbus:

- a. Hold Register Value. This is the 8-bit value that is loaded into the Sub-Revolution Delay Counter.
- b. Current Count Value. This is the 1sByte value of the Sub-Revolution Delay Counter. It is read on the fly and consecutive reads may yield different values. This value is used for diagnostic purposes.

### **3.2.4 Trigger Counter**

The Trigger Counter is a 32-bit count-down counter that is loaded from the trigger hold register with the required number of output pulses and whose clock input is the output of the Trigger Counter Clock Selector. This counter counts the number of trigger pulses output and can be set to any value from 1 to 4.29E9. The contents of the hold register are transferred to the counter on the occurrence of the Trigger Counter Terminal Count . The following value can be read via the VMEbus:

Hold Register Value. This is the 32-bit value that is loaded into the Trigger Counter.

### **3.2.5 Pulse Width**

The Pulse Width Counter is a 16-bit count-down counter that is loaded from the pulse width hold register with the required pulse width of all output pulses. It is enabled by the Sub-Revolution Counter Terminal Count.. This counter counts  $32 * \text{Frev}$ . The following value can be read via the VMEbus:

Hold Register Value. This is the 16-bit value that is loaded into the Pulse Width Counter and will determine the pulse width of the output pulse(s). The width can be set from 29.5ns (1) to 1.94ms (65536).

### **3.2.6 Fine Delay**

Fine Delay is accomplished through an external (relative to all other delays) silicon delay line. An 8-bit value is loaded into the Fine Delay hold register and the fine delay module. Resolution is 500ps. The delay is adjustable from 12ns (latency) to 139.5ns. (Input pulse width specifications need to be followed to realize the maximum delay.)

### **3.2.7 Timestamp**

The Timestamp is the 32-bit count-up counter that is reset on the occurrence of a user configurable Event. The value that is read is the most recent Timestamp Value. The Timestamp can be configured to count a configurable Event or 29.5ns clocks ( $1/(32 * \text{Frev})$ ) derived from the Event Link carrier frequency.

## **4.0 VME Memory Map**

**A16 Address Space** Boundary is selected via jumpers

<b>Address Range</b>	<b>Description</b>	<b>Valid Address / data modes</b>	<b>Size (used)</b>
<b>0000-003f</b>	VME ID	29,2d /D16,D08(OE)	64 bytes (32 odd bytes)
<b>0040-007f</b>	Board Configuration Registers	29,2d /D16,D08(OE)	16 bytes
<b>0100-01ff</b>	Event Mask RAM	29,2d /D16,D08(OE)	256 bytes
<b>0400-043f</b>	RESERVED		
<b>0440-047f</b>	Ch 1 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)
<b>0480-04bf</b>	RESERVED		
<b>04c0-04ff</b>	Ch 2 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)
<b>0500-053f</b>	RESERVED		
<b>0540-057f</b>	Ch 3 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)
<b>0580-05bf</b>	RESERVED		
<b>05c0-05ff</b>	Ch 4 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)
<b>0600-063f</b>	RESERVED		
<b>0640-067f</b>	Ch 5 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)
<b>0680-06bf</b>	RESERVED		
<b>06c0-06ff</b>	Ch 6 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)
<b>0700-073f</b>	RESERVED		
<b>0740-077f</b>	Ch 7 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)
<b>0780-07bf</b>	RESERVED		
<b>07c0-07ff</b>	Ch 8 Configuration Registers	29,2d /D16,D08(OE)	64 bytes (32 used)

The Trigger Module supports only single and double byte accesses (D16 and D08OE).

## 5.0 VME Memory and Register Definitions

### **5.1 VMEID**

The VMEID is resident in the first 32 odd bytes of the memory space. Total memory space allocated is 64 bytes. All bytes are read from the VME Interface gate array. The format for the VMEID is the standard format that has been used for all SNS VME boards.

### **5.2 Event Mask RAM**

The least significant byte of the event mask RAM address space represents each of the 256 possible event codes. Each of the 8 data bits in each event code address is used to determine whether an enable pulse should or should not occur on the respective output trigger channel. A bit value of 1 indicates that an enable pulse should be generated, and a bit value of 0 indicates that an enable pulse should not be generated. The following list defines the function of each bit in the event mask RAM.

### Event Mask RAM Bit Definitions

bit number	Function
0	Channel 1 Enable
1	Channel 2 Enable
2	Channel 3 Enable
3	Channel 4 Enable
4	Channel 5 Enable
5	Channel 6 Enable
6	Channel 7 Enable
7	Channel 8 Enable

If the Sub-Revolution Counter Enable Selector is selected to be an Event, the Revolution Counter Enable Selector will be ignored.

### 5.3 Board Configuration Registers

The following registers and bit assignments are global and affect all channels.

0040: rd/wr Command Register

bit 0 – Module Enable: set when configuration is complete

bit 1 – Ref/\*Auto: Ref Oscillator/LinkClk

0041: rd/wr Interrupt Level

bit 0-2 – Interrupt Level

0044: rd/wr Event Code for Revolution Frequency ReSync

0046: rd/wr Event Code for Timestamp Reset

004E: rd/wr RF Clock/Link Clock Delay

004F: rd/wr Text Event Code

0050: rd/wr PrePulse Event Code

0051: rd/wr T0 Event Code

### 5.4 Channel Configuration Registers

32 bytes of channel configuration data are allocated per channel as follows:

0440-045f Channel 1

04c0-04df Channel 2

0540-055f Channel 3

05c0-05df Channel 4

0640-065f Channel 5

06c0-06df Channel 6

0740-075f Channel 7

07c0-07df Channel 8

Channel control register and bit assignments are allocated for each of the eight channels and Channel 1 bit assignments are as follows :

0440: rd/wr Delay Control Register

- bit 0 - Reload Counters on Trigger Counter Terminal Count
- bit 1 – RESERVED
- bit 2 – RESERVED
- bit 3 - RESERVED
- bit 4 – VMEbus Trigger Command
- bit 5 – VMEbus Reset Command - Clears all counter and command Values
  - 0 = not Reset
  - 1 = Reset
- bit 6 - STOP - halts counting of all counters
  - 0 = Count
  - 1 = Stop
- bit7 - Output Polarity
  - 0 = Non-inverted
  - 1 = Inverted

0441: rd/wr Counter Control Register

- bit 1,0 – Revolution Delay Enable Selector
  - 00 – VMEbus
  - 01 – Event
  - 10 – External
  - 11 – Previous Channel (not Channel 1)
- bit 3,2 – Sub-Revolution Delay Enable Selector
  - 00 – VMEbus
  - 01 – Event
  - 10 – Revolution Delay Enable/Revolution Delay Counter Terminal Count
  - 11 – Revolution Delay Counter Terminal Count
- bit 5,4 – Halt Delay Clock Select
  - 00 – Fine Delay Clock
  - 01 – No Halt
  - 10 – Not Used
  - 11 – Next Channel (not Channel 8)
- bit 6 – Pulse Width Enable Select
  - 0 – Sub-Revolution Delay Counter Terminal Count
  
- bit 7 – Fine Delay Clock Select
  - 0 – Undefined
  - 1 – Variable Pulse Width

0443: rd Counter Status Flags

A 1 in any of the following bit locations indicates that the condition is true.

- bit 0 – Waiting for Revolution Delay Enable
- bit 1 – Waiting for Revolution Delay Terminal Count
- bit 2 - Waiting for Sub-Revolution Delay Enable
- bit 3 – Waiting for Sub-Revolution Delay Terminal Count
- bit 4 – Waiting for Trigger Terminal Count

0448: rd/wr msbyte Revolution Delay Hold Register

0449: rd/wr lsbyte Revolution Delay Hold Register

044b: rd lsbyte Revolution Delay Counter Value

044c:

044d: rd/wr lsbyte Sub-Revolution Delay Hold Register

044f: rd lsbyte Sub-Revolution Delay Counter Value

0450: rd/wr msbyte Trigger Hold Register

0451: rd/wr           Trigger Hold Register

0452: rd/wr           Trigger Hold Register

0453: rd/wr lsbyte   Trigger Hold Register

0454: rd/wr msbyte Pulse Width Hold Register

0455: rd/wr lsbyte Pulse Width Hold Register

0456: rd/wr Fine Delay Hold Register

0457:

0459: rd/wr Event Timestamp Code

045a: rd/wr Timestamp Configuration Register

- bit 0 – Timestamp on an Event
- bit 1 – Timestamp on First Output Pulse (of a series).
- bit 2 – Timestamp on Trigger Counter Terminal Count
- bit 3 – Timestamp Clock Source
  - 0 – 29.5ns (32 \* Frev) clock derived from the carrier frequency
  - 1 – an Event

045b: rd/wr Event Code for Timestamp Clock Source

045c: rd msbyte Timestamp Value

045d: rd           Timestamp Value

045e: rd           Timestamp Value

045f: rd lsbyte   Timestamp Value

## 5.5 VME Interface Registers

0042: rd/wr Interrupt Enable

- bit 0 - Channel 1 Trigger Terminal Count
- bit 1 - Channel 2 Trigger Terminal Count
- bit 2 - Channel 3 Trigger Terminal Count
- bit 3 - Channel 4 Trigger Terminal Count
- bit 4 - Channel 5 Trigger Terminal Count
- bit 5 - Channel 6 Trigger Terminal Count
- bit 6 - Channel 7 Trigger Terminal Count
- bit 7 - Channel 8 Trigger Terminal Count

0043: rd/wr Interrupt Enable

The interrupt is enabled when the corresponding bit is high.

- bit 0 -
- bit 1 -
- bit 2 -
- bit 3 - Event Link Carrier error
- bit 4 - Event Link Frame error
- bit 5 - Event Link Parity error
- bit 6 - Timestamp Reset Event
- bit 7 - Timestamp source

0045: rd Interrupt Status Register

This register indicates the cause of the interrupt.

When this register is read, the interrupt request on the VMEbus WILL be cleared. The interrupt status bit in this register will remain in a logic 1 state until the error condition is cleared. If the interrupt is caused by an Event Link Error, interrupt source register 0049 must be read to determine the actual cause of the interrupt. If a Channel Halt interrupt occurs, Interrupt source register 004b must be read to determine which Channel Halt occurred. If a Timestamp Trigger interrupt occurs, Interrupt Source Register 004d must be read to determine which channel timestamp occurred.

- bit 0 - reserved
- bit 1 - reserved
- bit 2 - reserved
- bit 3 – Event Link Error
- bit 4 – Channel Trigger Terminal Count
- bit 5 - reserved
- bit 6 - Timestamp Reset Event
- bit 7- Timestamp source

0047: rd/wr interrupt vector

- bit 0-7 – VME Interrupt Vector

#### 0048: rd Links Status

The bits in this register are identical to the interrupt status register, addr 0049. Reading this register will NOT cause the interrupt to be cleared. The front end computer may poll this register after an interrupt occurs to determine if the error condition still exists.

- bit 0 -
- bit 1 -
- bit 2 -
- bit 3 - Event Link Carrier error
- bit 4 - Event Link Frame error
- bit 5 - Event Link Parity error
- bit 6 - Timestamp Reset Event
- bit 7 -

#### 0049: rd Interrupt Source: Links

This register indicates the source of an interrupt. This register must be read by the interrupt handler if an Event Link or a Beam Sync Link Interrupt occurred. Reading this register will clear the Interrupt Source.

- bit 0 -
- bit 1 -
- bit 2 -
- bit 3 - Event Link Carrier error
- bit 4 - Event Link Frame error
- bit 5 - Event Link Parity error
- bit 6 - Timestamp Reset Event
- bit 7 -

#### 004a: rd Trigger Counter Terminal Count Status

The bits in this register are identical to the interrupt status register, addr 004b. Reading this register will NOT cause the interrupt to be cleared. The front end computer may poll this register after an interrupt occurs to determine if the channel is still in the Terminal Count state.

- bit 0 - Channel 1
- bit 1 - Channel 2
- bit 2 - Channel 3
- bit 3 - Channel 4
- bit 4 - Channel 5
- bit 5 - Channel 6
- bit 6 - Channel 7
- bit 7 - Channel 8

#### 004b: rd Interrupt Source: Trigger Counter Terminal Count

This register indicates the source of an interrupt. This register must be read by the interrupt handler if a Trigger Counter Terminal Count Interrupt occurred. Reading this register will clear the Interrupt Source.

- bit 0 - Channel 1
- bit 1 - Channel 2
- bit 2 - Channel 3
- bit 3 - Channel 4
- bit 4 - Channel 5
- bit 5 - Channel 6
- bit 6 - Channel 7
- bit 7 - Channel 8

#### 004d: rd Interrupt Source: Timestamp

This register indicates the source of an interrupt. This register must be read by the interrupt handler if a Timestamp Interrupt occurred. Reading this register will clear the Interrupt Source.

- bit 0 - Channel 1
- bit 1 - Channel 2
- bit 2 - Channel 3
- bit 3 - Channel 4
- bit 4 - Channel 5
- bit 5 - Channel 6
- bit 6 - Channel 7
- bit 7 - Channel 8

#### 004c: rd Timestamp Status

The bits in this register are identical to the interrupt status register, addr 004d. Reading this register will NOT cause the interrupt to be cleared. The front end computer may poll this register after an interrupt occurs to determine if the channel timestamp has been read.

- bit 0 - Channel 1
- bit 1 - Channel 2
- bit 2 - Channel 3
- bit 3 - Channel 4
- bit 4 - Channel 5
- bit 5 - Channel 6
- bit 6 - Channel 7
- bit 7 - Channel 8

## 6.0 Front Panel Connectors and Indicators

### **6.1 Front Panel Connectors**

### **6.1.1 Twin Axial**

The following input is provided via front panel twin axial connections:

Event Link (1)

### **6.1.2 LEMO**

Either of the following is jumper selectable and provided via front panel 2-conductor LEMO Model EGG Series 0B connector:

Recovered RF Clock (buffered) Output

Recovered Link Clock (buffered) Output

This output is a differential ECL level.

### **6.1.3 SMCP**

The following are provided via front panel single ended SMCP connectors:

External Trigger Inputs (4)

Trigger Outputs (8)

The External Trigger Inputs are TTL 50 ohms. The Trigger Outputs are TTL 50 Ohm drivers.

## **6.2 Front Panel Indicators**

VME Select – indicates a VME bus access to an address within memory space.

OFFLINE - indicates that the module has not been initialized.

Beam Synchronous Event Link – Carrier Active

External Trigger Inputs (4)

Channel Active (8)